Journal of Materials Chemistry C

ROYAL SOCIETY OF CHEMISTRY

PAPER

View Article Online
View Journal

Cite this: DOI: 10.1039/d1tc01451j

Synaptic transistors with human brain-like fJ energy consumption *via* double oxide semiconductor engineering for neuromorphic electronics†

Seong-In Cho, Jae Bum Jeon, Joo Hyung Kim, Seung Hee Lee, Wooseok Jeong, Jingyu Kim, Geunyoung Kim, Kyung Min Kim * and Sang-Hee Ko Park *

Received 30th March 2021,
Accepted 21st June 2021

DOI: 10.1039/d1tc01451j

rsc.li/materials-c

Neuromorphic devices that mimic a human brain have attracted significant attention in the field of next-generation semiconductors. The human brain can efficiently process information with low power consumption. Several energy efficient artificial synapses have been reported; however, the energy consumption of these synapses is significantly higher than that of the human brain (10 fJ). In this study, we propose the use of double oxide semiconductors for obtaining synaptic transistors with ultra-low energy consumption. The synaptic transistor comprising InZnO (IZO) and InGaZnO (IGZO) exhibits a high mobility and positive turn-on voltage, which are required for ultra-low energy consumption. SiO_2 deposited at 200 °C by plasma enhanced atomic layer deposition is used as an electric double layer gate insulator. The IZO/IGZO synaptic transistor consumed an ultra-low energy of 0.269 fJ (gate voltage: 3.5 V, 1 ms and drain voltage: 3 mV). Furthermore, the synaptic transistor exhibits various synaptic plasticity features under the brain-like energy conditions, including excitatory post-synaptic current, paired-pulse facilitation, potentiation, and depression. All of the operations of the devices were performed under ambient conditions (25 °C, humidity 50%), in the dark probe station. The IZO/IGZO synaptic transistor exhibits similar energy efficiency to a human brain, and this strategy is expected to be utilized for the fabrication of various ultra-low energy consuming synaptic transistors.

Introduction

Next-generation computing beyond the conventional Von Neumann architecture has recently attracted significant interest in semiconductor research with the goal of low power computing. One of the technologies of interest is the so-called "neuromorphic computing" device that mimics the low power consumption of the human brain.[1–3] The brain, despite its complex network comprising 100 billion neurons and 100 trillion synapses, has an exceptionally efficient energy consumption of 20 W.[4,5] To realize that efficiency, the energy consumption per single synapse unit must be below 10 fJ.[5]

To simulate the human brain, the key requirement is the development of an artificial synaptic element that shows an analog conductance change characteristic with respect to the amount and polarity of the external electrical stimuli.[6] In addition, low power operation capability with power usage like that of the biological synapse is crucial. Two types of devices are potential artificial synapse candidates: a two-terminal device with a capacitor structure and a three-terminal device with a transistor structure. Previously, the two-terminal devices, known as "memristors," have been intensively investigated for their application as artificial synapses.[7–12] These devices could approximate synaptic functions in the simplest configuration, favourably realizing the highest density at the given feature size. However, this design intrinsically suffers from a high energy consumption issue because of the lack of selecting units that eliminate sneak currents. Alternatively, three-terminal synaptic devices have been proposed, wherein the separation of the programming and reading terminals deal with the sneak current issues and guarantee better robustness.[13–19] In a three-terminal synaptic device, the reversible change of the gate insulator (GI) property can induce hysteresis in the transfer curve, resulting in the change in conductance of the channel. The resistance change shown through hysteresis suggests that the three-terminal device can express 0 and 1 or multi-levels as a memory device or an

Department of Materials Science and Engineering, Korea Advanced Institute of Science and Technology (KAIST), 291 Daehak-ro, Yuseong-gu, Daejeon 34141, Republic of Korea. E-mail: km.kim@kaist.ac.kr, shkp@kaist.ac.kr

† Electronic supplementary information (ESI) available. See DOI: 10.1039/d1tc01451j

artificial synapse.[20–22] Various mechanisms have been reported for the GI, such as mobile ion conducting, electron or proton trapping, and ferroelectric polarization.[13–15,17,23]

Thin-film transistors (TFTs) based on amorphous oxide semiconductors (AOSs), known as oxide TFTs have been reported as effective low energy consuming neuromorphic devices.[24–26] The energy consumption per spike event (W) of synaptic transistors is obtained using the following equation:

$$W = I_{peak} \times t \times V_{DS}$$

where I_{peak}, t, and V_{DS} are the peak excitatory post-synaptic current (EPSC), pulse width, and drain voltage, respectively.[24,27–30] This equation indicates that a synaptic transistor must be able to generate a distinct signal of low current even with a low V_{DS} to achieve an ultra-low driving energy. Due to the special energy band structure of AOSs, oxide TFTs exhibit extremely low off-current and relatively high mobility. Several studies have been conducted to apply these properties in various electronics such as displays and memory devices.[31–34] For example, in displays oxide TFTs have already been successfully mass-produced, and J. Rosa *et al.* reported oxide semiconductor based resistive memory devices.[35] Furthermore, G. J. Jeon *et al.* introduced a fingerprint sensor based on oxide TFTs.[36] These great properties of oxide semiconductors can also be utilized for neuromorphic devices because the low off-current and high mobility of oxide TFTs result in a low current signal of synaptic transistors and low V_{DS}, respectively. Several low energy consuming artificial synaptic devices have been reported; however, the energy consumption of these synapses ranges from nJ to pJ.[24–26,37–41]

Certain limitations have hindered the practical applications of AOSs in low energy consuming synaptic devices. Paradoxically, the unique energy band structures of the AOSs endow oxide TFTs with high mobility and low off-current, and they also cause some problems. High mobility and positive turn-on voltage (V_{on}) values are required to realize low energy driving by oxide TFTs. Mobility is an important parameter for producing current at a low voltage, and to lower the current level, a positive V_{on} value is required. A slight shift in V_{on} can result in several order differences in the current value because of the very low subthreshold swing value. In addition, high mobility is important not only for fast computation, but also for low energy consumption. However, both requirements depend on the carrier concentration of AOSs.[33] At high carrier concentration, the mobility of oxide TFT increases, but V_{on} shifts to a negative value. Therefore, controlling the partial oxygen pressure or thickness of the active layer cannot be used to address this trade-off.[42,43] Guo *et al.* implemented low power oxide neuromorphic transistors by reducing the active layer thickness and shifting the threshold voltage to a positive value; however, the mobility decreased as the threshold voltage became positive.[30] This trade-off relationship of AOS due to its unique band structure is a stumbling block for achieving low energy consumption. In addition, no study has provided detailed guidelines on the fabrication of energy efficient synaptic transistors.

Herein, we propose a multi-layered stack structure of synaptic transistors to reduce the energy consumption by maximizing the advantages of AOSs using double oxide semiconductors. We fabricated a synaptic transistor using double oxide semiconductors comprising InZnO (IZO) and InGaZnO (IGZO). In addition, an electric double layer (EDL), which has attracted significant attention as a high capacitance material for imitating synaptic plasticity, was used as the GI of the synaptic transistor.[13,14] Low temperature plasma enhanced atomic layer deposition (PEALD) of SiO_2 acts as an EDL GI. By applying voltage an EDL formed spontaneously at the interface between the electrolyte and conductor. The fabricated IZO/IGZO synaptic transistor exhibited an ultra-low energy consumption per spike of 0.269 fJ, which is lower than a human brain. In addition, the synaptic transistor exhibited various kinds of synaptic plasticity under the brain-like energy condition, including EPSC, paired-pulse facilitation (PPF), potentiation, and depression.

The high performance was obtained by using an optimized material design and fabrication process of the GI and the active layers. A detailed discussion of the material optimization, including an in-depth examination of the underlying mechanism, is provided below.

Results and discussion

Fig. 1a shows the structure of the ultra-low energy consumption synaptic transistor. Fig. 1b shows the ultra-corrected-energy-filtered-transmission electron microscopy (UC-EF-TEM) image of the fabricated synaptic transistor. Because the annealing process is conducted directly on the active layers, we fabricated the synaptic transistors with a top-gate structure. This top-gate bottom-contact (TGBC) structure is ideal for the fabrication of complex connections and can be developed into self-aligned synaptic transistors.[44,45] Fig. 1c illustrates the operation mechanism of the proposed synaptic device compared to the biological synapse. The gate electrode of the TFT is considered as the pre-synapse terminal, while the region containing the source/drain (S/D) electrodes and active layers are regarded as the post-synapse terminal. The conductance of the active layer is regarded as the synaptic weight, where the proton is the medium inducing the weight change as K^+ and Na^+ ions of the biological synapse. Consequently, the change in amount of drain current (I_{DS}) flowing represents the synaptic plasticity.

Gate insulator as a hydrogen reservoir with a barrier

The EDL-based GI in the synaptic transistor should possess several properties in order to serve as a H reservoir as well as the insulator. First, the GI itself should contain a high concentration of H. These H atoms can be transformed into mobile H^+ ions which form an EDL under an external electric field.[46] Secondly, the H inside the GI should be kept stable so it does not leak into the surrounding layers during fabrication. Incorporation of excess H inside the oxide semiconductor can be an origin of the degradation of the oxide TFT. Thirdly, leakage current should be as low as possible for the ultra-low power operation. Otherwise, the leakage current may overwhelm the operating power and thus, the low power operation

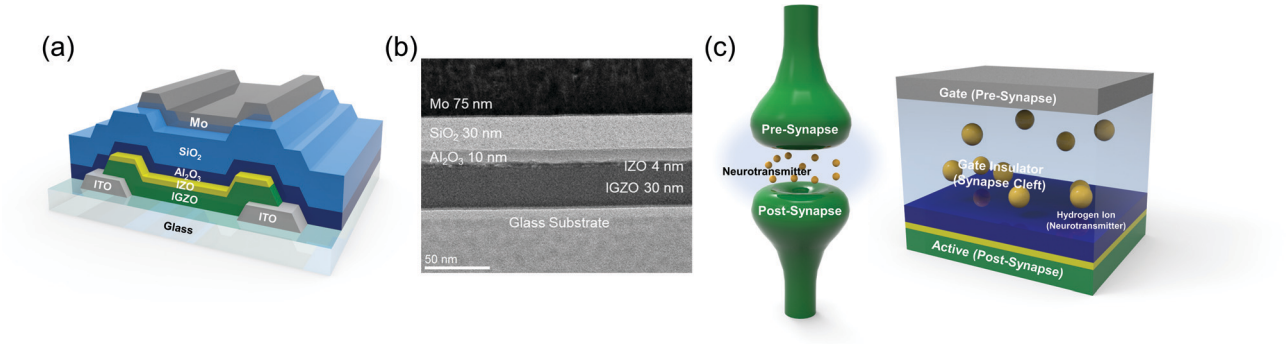

Fig. 1 (a) Schematic of the synaptic transistor with the proposed strategy for ultra-low energy consumption. (b) UC-EF-TEM image of the synaptic transistor with the proposed strategy for ultra-low energy consumption. (c) Schematic for comparison between a biological synapse and the synaptic transistor.

cannot be possible. In previous reports, including those regarding polymer- or ionic liquid-based synaptic transistors, leakage current typically occurred in the order of nA at a gate voltage (V_{GS}) lower than 5 V.[26,47–50] This level of leakage current is too high for the ultimate low power operation. In addition, since an EDL containing H^+ ions is affected by hydroxyl groups, it is important to always maintain the same environment including temperature and humidity. In this experiment temperature and humidity were maintained at 25 °C and 50%, respectively.

We found that the 200 °C-PEALD SiO_2 is the optimal EDL to meet the requirements of serving as a H reservoir. To investigate the properties of the 200 °C-PEALD SiO_2, we compared it to a 300 °C-PEALD SiO_2, which is a conventional insulator. To conduct capacitance–frequency (C–F) measurements, Metal–Insulator–Metal (MIM) devices with SiO_2 were fabricated. InSnO (ITO) was used as the bottom electrode and Mo was used as the top electrode. As shown in Fig. 2a, 30 nm of 200 °C-PEALD SiO_2 and 300 °C-PEALD SiO_2 showed different C–F measurement results. The 200 °C-PEALD SiO_2 exhibited a large maximum specific capacitance of 0.33 μF cm^{-2}, which is significantly larger than that of 300 °C-PEALD SiO_2. Due to polarization of H^+ ions, this large capacitance value is measured.[49,51] In addition, unlike the 300 °C-PEALD SiO_2, the 200 °C-PEALD SiO_2 exhibited a frequency-dependent capacitance, which is the most important characteristic of a suitable EDL. These observations indicate that the 200 °C-PEALD SiO_2 is significantly different from other conventional insulators and exhibits EDL properties.

To further investigate these unique properties of the 200 °C-PEALD SiO_2, various microscopic analyses were conducted. Fig. S1a and b (ESI†) show the X-ray reflectivity (XRR) results

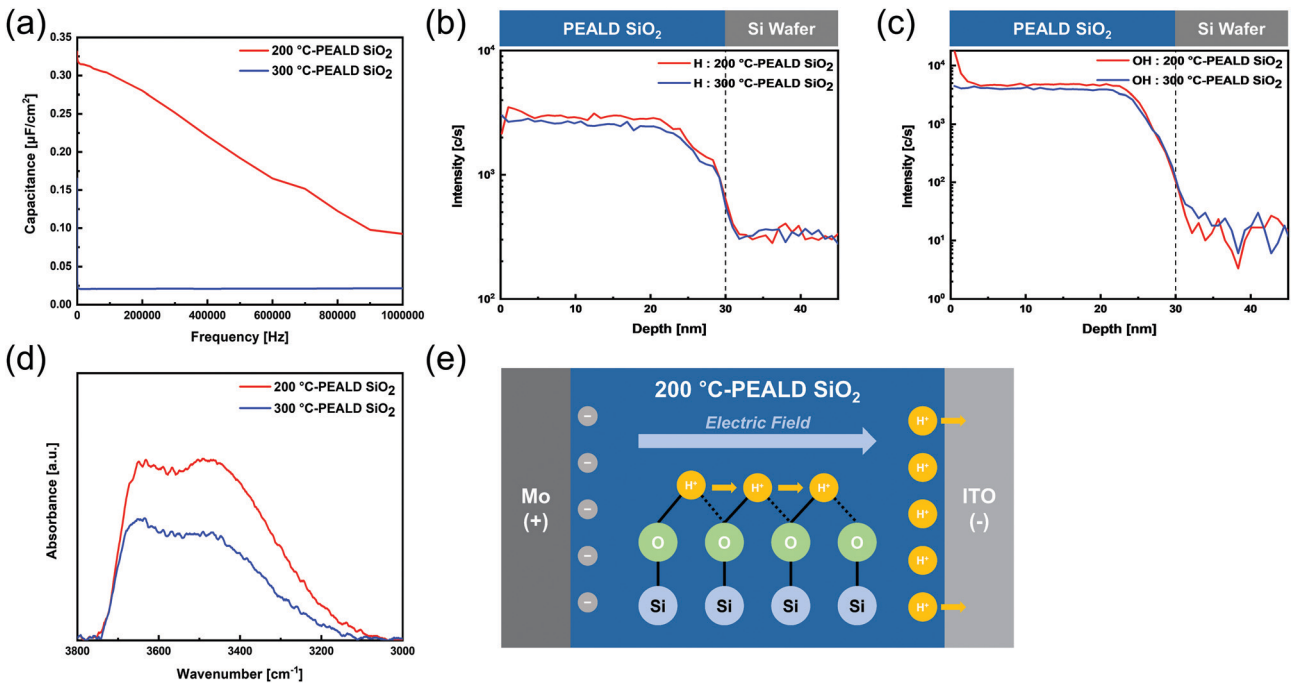

Fig. 2 Comparisons between PEALD SiO_2 at deposition temperatures of 200 °C and 300 °C by (a) C–F measurement. The SIMS results of (b) H and (c) OH elements, as well as (d) FT-IR spectroscopy. (e) H^+ ion conducting mechanism of 200 °C-PEALD SiO_2.

of both the 200 °C- and 300 °C-PEALD SiO_2. The density of the 200 °C-PEALD SiO_2 was 2.15 g cm^{-3}, which is lower than that of the 300 °C-PEALD SiO_2 (2.40 g cm^{-3}). This can be attributed to the faster deposition rate (0.138 nm per cycle) at 200 °C compared to that at 300 °C (0.114 nm per cycle). Typical temperature-dependent characteristics of the ALD process seem to apply, where the lower energy of the precursors results in incomplete surface reactions at low temperatures, leading to less dense film formation and a faster deposition rate. The low surface reactivity suppresses the full chemisorption between the –OH termination on the surface and the Si precursor (Bisdiethylamino silane, BDEAS), causing the –OH groups to remain on the surface. Eventually, the low temperature deposited SiO_2 film can include a higher concentration of H acting as the mobile species and forming the EDL. The secondary ion mass spectrometry (SIMS) analysis results of H and OH elements confirm that the 200 °C-PEALD SiO_2 has higher H and OH concentrations than 300 °C-PEALD SiO_2 (Fig. 2b and c). Fig. 2d shows the Fourier-transform infrared (FT-IR) spectra, which suggest the bonding state of the H impurities. The broad spectrum across the 3000–3700 cm^{-1} region corresponds to the –OH bond stretching vibration. The 200 °C-PEALD SiO_2 showed a higher –OH peak intensity than the 300 °C-PEALD SiO_2.[52]

Based on the previous result, the H^+ ion conducting mechanism of 200 °C-PEALD SiO_2 was proposed, as shown in Fig. 2e. Briefly, the H incorporated in SiO_2 formed –OH groups, which become the origin of the mobile H^+ ions. When an external electrical field is applied across the 200 °C-PEALD SiO_2, the weakly bonded H splits out from one oxygen and jumps to another oxygen along the electric field. Consequently, these mobile H^+ ions accumulate at the interface between SiO_2 and the ITO electrode by the Grotthuss mechanism.[49,51,53,54] These mobile ions participate in polarization together with electrons to induce a large, frequency-dependent capacitance, which was not observed in the 300 °C-PEALD SiO_2. In addition, some mobile ions may penetrate into ITO under a strong electric field.

During the GI deposition, the H can be easily incorporated into the AOS and deteriorate the conductivity of the channel.[55] Several studies have reported that H acts as a shallow donor in oxide semiconductors and makes TFTs conductive.[56,57] When the 200 °C-PEALD SiO_2 was directly deposited on IZO, the TFTs became conductive regardless of thickness, as shown in Fig. S2 (ESI†). Therefore, the 200 °C-PEALD SiO_2 cannot be applied directly to the synaptic transistors.

One of the possible solutions is the insertion of a H barrier layer underneath the EDL. For that purpose, we adopted a PEALD Al_2O_3. This material is well-known for its excellent H barrier property, having a lower H concentration compared to the thermal-ALD Al_2O_3.[58,59] To investigate the optimum thickness of the barrier layer, we performed C–F measurements for the 30 nm-thick SiO_2/10 nm to 30 nm-thick Al_2O_3 capacitor structure, as shown in Fig. S3b (ESI†). The thinner Al_2O_3 (10 nm) MIM exhibited a larger maximum specific capacitance value (0.17 μF cm^{-2}) and a greater frequency dependency compared to other thicknesses. As will be mentioned later, unlike when there is no H barrier, when there is 10 nm-thick Al_2O_3, the on/off characteristic is shown, and only 10 nm is enough for the H barrier. Therefore, we designed synaptic transistors with a double GI composed of a 10 nm-thick H barrier and a 30 nm-thick EDL. Fig. S3c (ESI†) shows the leakage current of the synaptic transistor with 30 nm-thick SiO_2 and 10 nm-thick Al_2O_3. The leakage current with response to a V_{GS} of 5 V was 9.16 pA, which is an extremely low value compared to those of other reported EDL TFTs.[26,47–50] The SiO_2/Al_2O_3 GI structure that we designed completely satisfies all the requirements of the desired type of synaptic transistor.

IZO/IGZO double oxide semiconductors for ultra-low energy consumption

To be used in an ultra-low energy driving synaptic device, a synaptic transistor must exhibit specific characteristics in the transfer curves. First, its mobility should be high for lower voltage current induction. Second, V_{on} must be larger than 0 V for mimicking synaptic plasticity at low current. The V_{on} is defined as V_{GS} where I_{DS} reaches 20 pA ((width/length) × 10 pA). It is difficult to achieve both requirements in oxide TFT. For higher mobility, the carrier concentration should be high. However, a high carrier concentration also shifts the V_{on} to a negative value. In addition, there should be enough hysteresis between the forward and back sweep to induce the analogical change of conductance of the active layer for a given V_{DS}.

To satisfy the requirements, we adopted an IZO/IGZO double-layer stack for the active layer. Fig. 3a–c show the transfer curves of synaptic transistors with IZO-only, IZO/IGZO double oxide semiconductors, and IGZO-only, respectively. The forward sweep was first conducted by increasing the V_{GS} from −5 to 5 V, followed by the back sweep, which included decreasing the V_{GS} from 5 to −5 V. The V_{DS} was fixed to 0.003 V during all electrical measurements. This V_{DS} is acceptably low, if synaptic plasticity can be mimicked.[27,28]

Table 1 summarizes the electrical properties of the synaptic transistors extracted from the transfer curves and Hall measurements. A counter-clockwise hysteresis was obtained for all devices.[21] The IZO-only synaptic transistor, which has the highest carrier concentration, exhibited the highest field-effect mobility of 63.70 $cm^2 V^{-1} s^{-1}$. However, due to its high carrier concentration, the V_{on} value was negative (−1.90 V), making it unsuitable for use as an energy-efficient synaptic transistor. In contrast, the IGZO-only synaptic transistor with the lowest carrier concentration exhibited a positive V_{on} value (4.33 V), however, owing to its extremely low mobility (1.99 $cm^2 V^{-1} s^{-1}$), it exhibited a poor on/off characteristic under a low V_{DS} of 0.003 V. Meanwhile, the IZO/IGZO synaptic transistor possesses the advantages of both IZO and IGZO and shows an ideal transfer curve for ultra-low energy driving synaptic TFT. Although its carrier concentration was one order below that of IZO, its mobility was as high as that of IZO (59.04 $cm^2 V^{-1} s^{-1}$). In addition, it showed an ideal V_{on} of 0.70 V owing to the balanced V_{on} between the IZO and IGZO. The excellent device-to-device uniformity is shown in Fig. S4 (ESI†).

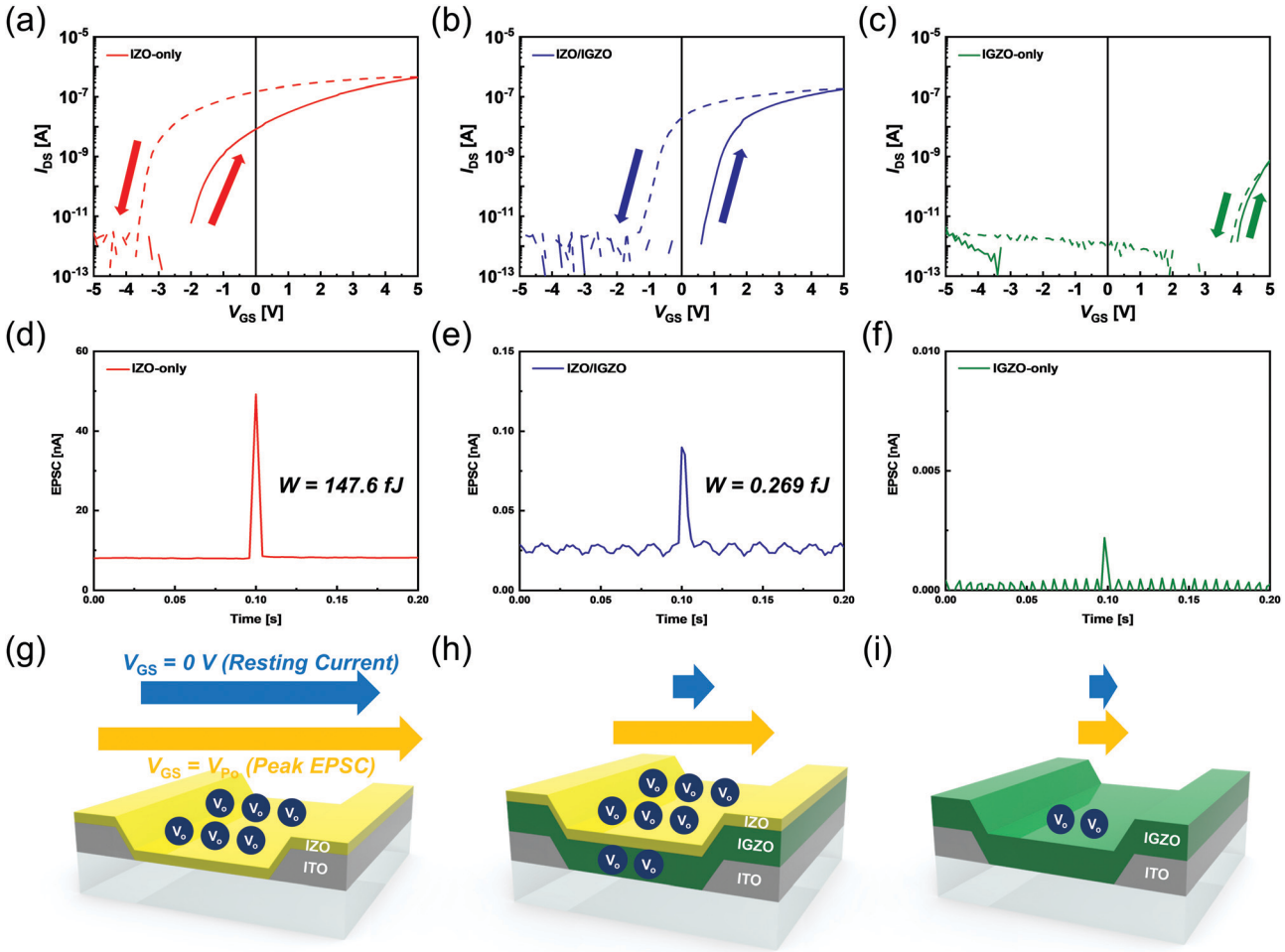

Fig. 3 Transfer curves of (a) IZO-only, (b) IZO/IGZO, and (c) IGZO-only synaptic transistors. Solid lines represent forward sweeps and dashed lines represent reverse sweeps. The EPSC characteristics of (d) IZO-only, (e) IZO/IGZO, and (f) IGZO-only synaptic transistors (V_{DS} = 0.003 V). Schematic diagrams of current flowing through (g) IZO-only, (h) IZO/IGZO, and (i) IGZO-only synaptic transistors in each situation.

Table 1 Electrical properties of synaptic transistors with different active layers

Active layer	IZO-only	IZO/IGZO	IGZO-only
Field-effect mobility [$cm^2\ V^{-1}\ s^{-1}$]	63.70 ± 1.13	59.04 ± 0.63	1.99 ± 0.27
Subthreshold-swing [V per decade]	0.64 ± 0.38	0.21 ± 0.06	0.20 ± 0.11
Hysteresis [V]	−1.80 ± 0.10	−1.76 ± 0.14	−0.17 ± 0.07
V_{on} [V]	−1.90 ± 0.20	0.70 ± 0.10	4.33 ± 0.13
Carrier concentration [cm^{-3}]	3.03×10^{19}	5.85×10^{18}	4.13×10^{16}

The output curves under a V_{GS} of 3.5 V are shown in Fig. S5 (ESI†).

These differences in transfer and output curves directly affect synaptic properties and energy consumption. The potentiation voltage (V_{Po}) was 3.5 V. The pulse duration time was fixed at 1 ms, similar to a human brain.[13] The values were obtained under a low V_{DS} of 0.003 V. The EPSC characteristic of the IZO-only synaptic transistor is shown in Fig. 3d. The IZO-only synaptic transistor exhibited a high resting current and EPSC peak of 7.98 and 49.2 nA, respectively. Owing to its negative V_{on} value, the IZO-only synaptic transistor operated under normally-on mode. In other words, although a voltage of 0 V was applied to the gate electrode, the current flowed, which corresponded to the resting current. Consequently, the IZO-only synaptic transistor exhibited a high current order and consumed a relatively high energy per event of 147.6 fJ. Although this energy consumption value is competitive compared to the previously reported synaptic devices, it is still significantly higher than that of a human brain. Fig. 3f shows the EPSC characteristic of the IGZO-only synaptic transistor. In contrast, the IGZO-only synaptic transistor operated under normally-off mode; therefore, the off-current corresponded to the resting current. The resting

current and peak EPSC of the IGZO-only synaptic transistor were almost noise level at 0.32 and 2.19 pA, respectively. The peak current was induced, but because of its extremely low mobility, an extremely low peak current flowed at a low V_{DS} of 0.003 V. This peak EPSC is meaningless because the gate leakage current under a V_{GS} of 3.5 V was approximately 4.9 pA, which is higher than the peak EPSC under the same V_{GS} condition. At the V_{GS} corresponding to the V_{Po}, the IGZO synaptic transistor is in the off state, and the off-current is very low, so it seems that the EPSC peak is lower than the leakage current. In addition, because of its low mobility and poor current characteristic, it is difficult to determine if the IGZO-only synaptic transistor induced a change in the conductance of the active layer under low voltage. Fig. 3e shows the EPSC characteristic of the IZO/IGZO synaptic transistor. Like the IGZO-only synaptic transistor, the IZO/IGZO synaptic transistor operated under normally-off mode, and thus, its resting current was quite low (26.3 pA). This value almost corresponded to the off-current, which was near to 20 pA, where the V_{on} is defined. In addition, like the IZO-only synaptic transistor, it showed a distinct EPSC peak (89.8 pA) under low V_{DS} owing to its high mobility. For this instance, because the EPSC was significantly larger than the gate leakage current, the gate leakage current can be ignored. This IZO/IGZO synaptic transistor exhibited an ultra-low energy consumption of 0.269 fJ. Fig. 3g–i show the schematic diagrams of current flowing for all cases in each situation. The blue and orange arrows represent the amount of current at V_{GS} = 0 V and V_{GS} = V_{Po}, respectively. They also display the oxygen vacancy (V_o) density relatively in IZO and IGZO layers which are associated with the V_{on}. This result was achieved by utilizing the advantages of both the low off-current and high mobility of the oxide semiconductors, and it shows that the proposed strategy for fabricating an ultra-low energy consuming transistor is effective.

To confirm the mechanism of these electrical properties of the double oxide semiconductor synaptic transistor, an X-ray photoelectron spectroscopy (XPS) depth profile was obtained.

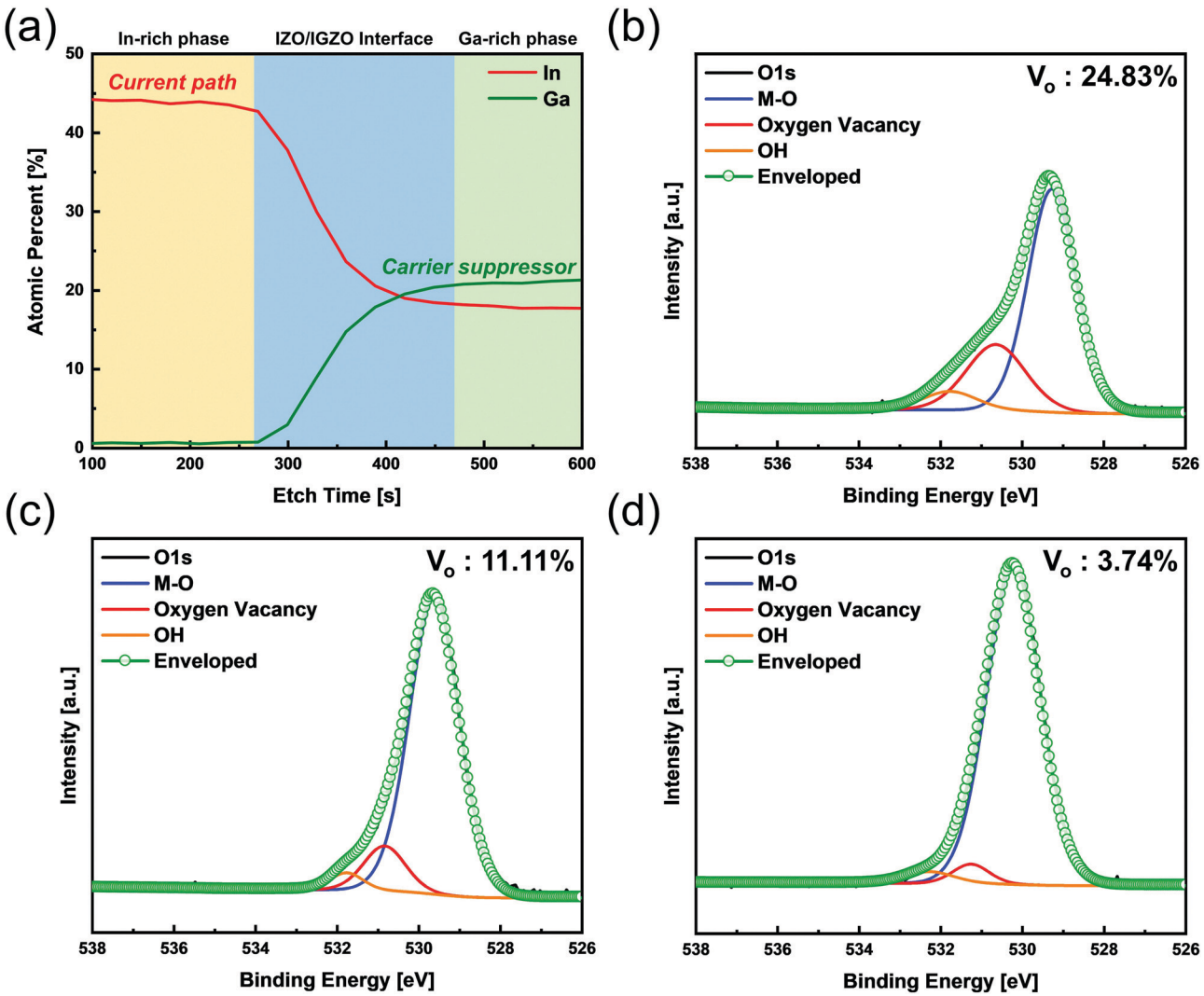

Fig. 4 (a) XPS depth profile result of IZO and IGZO double oxide semiconductors. Deconvoluted O1s peaks of each phase of annealed IZO and IGZO double oxide semiconductors: (b) In-rich phase, (c) IZO/IGZO interface, and (d) Ga-rich phase.

Fig. 4a shows the atomic distribution of In and Ga inside the IZO and IGZO layers. The IZO and IGZO layers comprised three parts, including the In-rich phase, IZO/IGZO interface, and Ga-rich phase. The Ga from IGZO acted as a carrier suppressor by forming a very strong bond with oxygen to suppress the formation of V_o, which acts as a shallow donor in AOS.[60] Owing to the supply of Ga from IGZO, the carrier concentration was reduced compared to that of the IZO-only, and the V_{on} value was shifted by −1.90 V to the desired positive value (0.70 V). The effect of Ga was verified by the Hall measurement results. The IZO/IGZO exhibited a lower carrier concentration (5.85×10^{18} cm^{-3}) than the IZO-only (3.03×10^{19} cm^{-3}). In contrast, despite the Ga supplement, the electron-accumulation channel region at the interface between the insulator and the active layer remained as an In-rich phase. In contrast to Ga, In formed a weak bond with oxygen, increasing the V_o generation and providing a carrier transport path in the oxide semiconductor by increasing the carrier concentration.[60,61] To determine the V_o concentration according to this atomic distribution, the O1s peaks in each region were deconvoluted. As shown in Fig. 4b, a shoulder peak can be observed in the O1s peak of the channel forming region, and the V_o concentration was relatively high (24.83%). In contrast, as shown in Fig. 4c and d, at the IZO/IGZO interface and Ga-rich phase, the V_o concentration was 11.11% and 3.74%, respectively. In addition, there was a decrease in the V_o concentration gradient from the front to the back channel. Accordingly, the binding energy of the metal–oxygen (M–O) bonding increased from 529.27 to 53.22 eV. The XPS results show that the IGZO located at the back channel of the double oxide semiconductors acted as a "carrier suppressor," thereby lowering the carrier concentration of the active layer and shifting the V_{on} to a positive value. In fact, when comparing IZO-only and the IZO/IGZO bilayer, it was confirmed by Hall measurement that the carrier concentration differed by

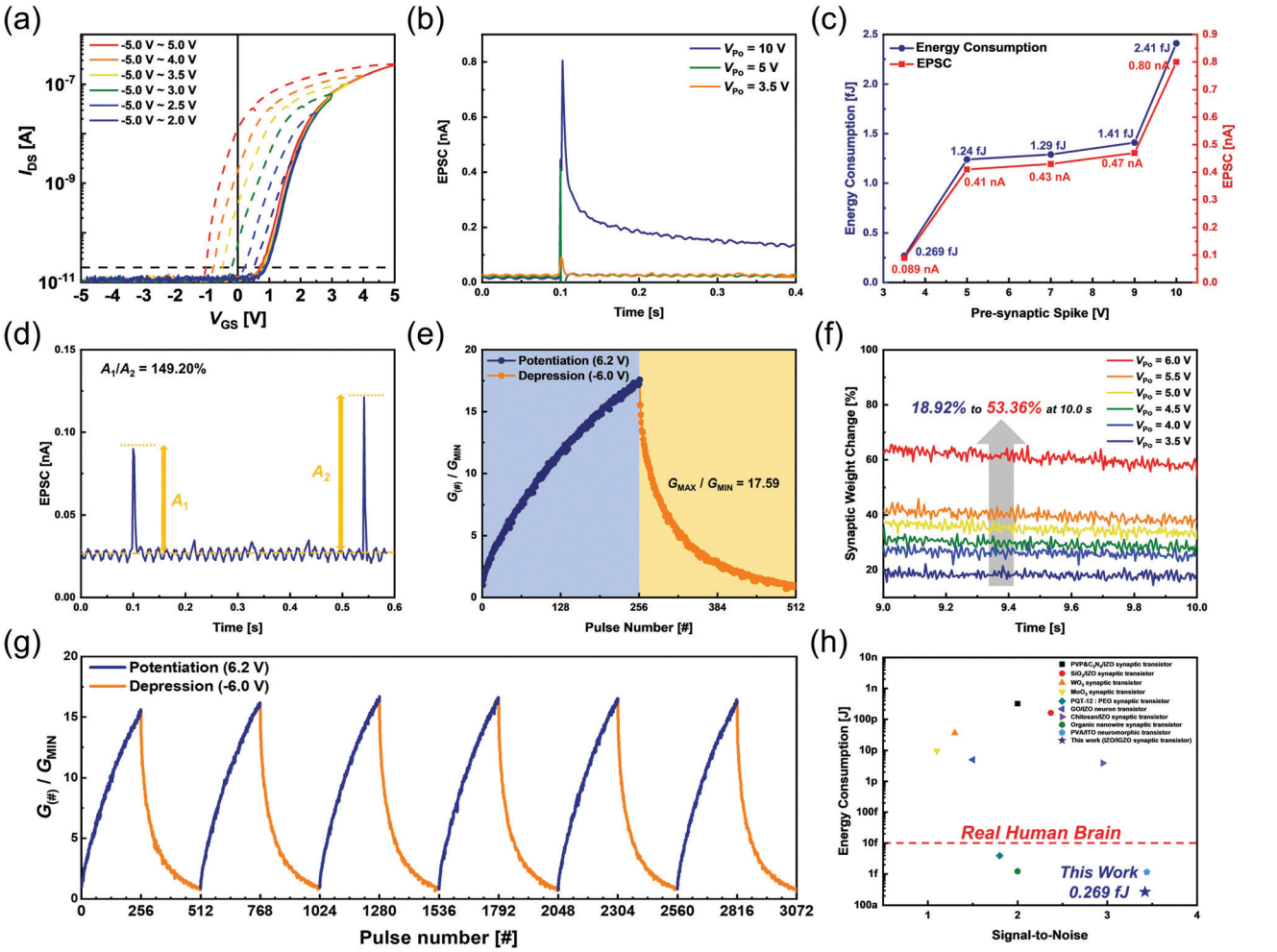

Fig. 5 (a) Transfer curves with different ranges of voltage sweep range (V_{DS} = 0.003 V). Synaptic plasticity of the IZO/IGZO synaptic transistor. (b) EPSCs of the IZO/IGZO synaptic transistor with different amplitudes of pre-synaptic spikes. (c) Energy consumption and EPSC peak values with different pre-synaptic spikes amplitudes. (d) PPF characteristic of the IZO/IGZO synaptic transistor. (V_{Po} = 3.5 V) (e) Potentiation and depression characteristics simulated by the IZO/IGZO synaptic transistor. (f) Synaptic weight change after potentiation with different amplitudes of pre-synaptic spikes. (g) Repetition characteristics of potentiation and depression emulated by the IZO/IGZO synaptic transistor (V_{DS} = 0.003 V). (h) Comparison of energy consumption with previously reported neuromorphic devices.

one order. Since V_{on} of the oxide TFT largely depends on the carrier concentration of the active layer, the positive V_{on} value of an IZO/IGZO synaptic transistor can be interpreted as proper tuning due to the presence of IGZO. On the other hand, the channel region at the front channel maintained a high V_o concentration like IZO and acted as the ''current path''. The field-effect mobility maintained a high value similar to that of the IZO-only device.

Synaptic plasticity simulated by IZO/IGZO synaptic transistors

Although low voltage and low current peak are induced, if synaptic plasticity cannot be mimicked at that voltage and current level, it is difficult to judge whether a device is an appropriate artificial synapse. The IZO/IGZO synaptic transistor displays various properties of synaptic plasticity that other EDL synaptic transistors can perform, even under brain-like energy conditions.[13] Fig. 5a shows the hysteresis analog characteristic at various maximum sweep voltages. As the measurement range widens, the hysteresis increases analogously. This implies that the transistor is capable of analog resistance changes and can mimic synaptic plasticity.

Fig. 5b shows the EPSC characteristics of the IZO/IGZO synaptic transistor at various pre-synaptic spikes. With an increase in the V_{Po} from 3.5 to 10 V, the EPSC peaks collectively increased from 0.089 to 0.80 nA. This value is similar to that of a human brain, particularly because a stronger input signal induced a larger output signal. In addition, the energy consumption increased from 0.269 to 2.41 fJ, as shown in Fig. 5c. Although the V_{GS} is not included in the energy consumption calculation formula, an increase in the V_{GS} causes an increase in the current and thus the energy consumption. Because the current level itself was extremely low, even with a strong pre-synaptic spike, the energy consumption was maintained at a human brain-like level. The PPF characteristic of the IZO/IGZO synaptic transistor is shown in Fig. 5d. The PPF is a short-term plasticity phenomenon, and it is considered essential for computing temporal information, such as auditory or visual signals in biological neural systems.[62] The V_{Po} was 3.5 V and the interval time between pulses was 0.44 s. The PPF index was calculated by the ratio between the first response (A_1) and the second response (A_2). The A_1 and A_2 values were 63.57 and 94.84 pA, respectively, and the PPF index (A_1/A_2) was 149.20%. If the interval time is short enough, the second pulse is applied before the mobile ion relaxation inside the EDL, which causes more ions to accumulate at the interface than the first pulse. In other words, more electrons accumulate to form a channel, and more current flows than in the previous pulse, making it possible to mimic various synaptic plasticity properties including PPF.[13,14,63,64]

Fig. 5e shows the potentiation and depression simulated by the IZO/IGZO synaptic transistor. The V_{GS} for reading was 1.5 V. During the application of pulses 256 times, the synaptic weight increased analogously. After applying these pulses, the synaptic weight reached a maximum (G_{MAX}). The IZO/IGZO synaptic transistor exhibited a large ratio between the G_{MAX} and minimum synaptic weight (G_{MIN}) of 17.59 with 256 levels of conductance states. Long-term depression (LTD) was also obtained by applying voltage of the opposite sign until the initial state was finally reached.[13] Fig. 5f shows the retention characteristic of different states, showing a concurrent of short-term memory (STM) and long-term memory (LTM), after different pre-synaptic voltages. At a low programming V_{GS} of 3.5 V, only 18.92% of the LTM component remained, while 53.36% remained at a V_{GS} of 6.0 V. Such STM and LTM characteristics of the IZO/IGZO synaptic transistor are comparable to those of the human brain as the memory retention is proportional to the intensity of the stimuli. The STM and LTM can be understood as follows. The positive V_{GS} application pushes H^+ ions to the GI/IZO interface. These accumulated H^+ ions accumulate more electrons at the channel. The H^+ ions relax slowly into the initial state by diffusion, resulting in the volatile conductance change. However, if the voltage signal is strong enough, some of the H^+ ions penetrate into the oxide semiconductor.[13] These penetrated H^+ ions cause an electrochemical doping effect on the oxide semiconductor.[65] The H^+ ions are well-known shallow donors of the oxide semiconductor, and these penetrated H^+ ions can induce long-term potentiation (LTP).[66,67] Since the stronger gate voltage allows more H^+ ions to penetrate through the oxide semiconductor, it induces larger LTP and displays behaviour similar to the human brain. Hysteresis window of an IZO/IGZO synaptic transistor as a function of endurance cycles is shown in Fig. S6 (ESI†). The hysteresis was measured by dual sweeping the V_{GS} from −5 to 5 V, the same as the previous measurement. In the first sweep, hysteresis of −1.9 V was observed, and in the subsequent sweeps repeated up to 100 times, the hysteresis was stably maintained around −2.2 V. Fig. 5g shows reproducible potentiation and depression characteristics over 6 cycles, with 3072 pulses. During repeated measurements, the cycle-to-cycle variation was only 3.91%. Thanks to maintaining stable hysteresis, even after several cycles, repeated potentiation and depression could be stably implemented. As previously mentioned, the synaptic plasticity is meaningful because it was driven under brain-like energy conditions.

Fig. 5h summarizes the benchmarking results of the energy consumption in major TFT-based synaptic devices reported so far, including the IZO/IGZO synaptic transistor described in this research.[25–27,30,38,39,41,65,68,69] The proposed double oxide semiconductor synaptic transistor exhibited excellent performance when compared to other oxide semiconductor-based devices, as well as other organic semiconductor, 2D material, and carbon nanotube-based devices. Only a few synaptic transistors showed comparable energy consumption to the human brain, our device included. To our knowledge, the energy consumption of the IZO/IGZO synaptic transistor in this study is the lowest reported value to date. From this viewpoint, it can be confirmed that using double oxide semiconductors is a promising strategy in human brain-like energy consuming synaptic transistors.

Conclusions

We fabricated an IZO/IGZO double oxide semiconductor-based neuromorphic transistor with ultra-low energy consumption, which is comparable to that of a human brain. Because of the enhancement mode (V_{on} 0.70 V) and high mobility

($59.04\ cm^2\ V^{-1}\ s^{-1}$) of the IZO/IGZO synaptic transistor, the minimum energy consumption of the transistor was 0.269 fJ. In addition, the IZO/IGZO synaptic transistor emulated synaptic plasticity, exhibiting properties such as EPSC, PPF, potentiation, and depression under the brain-like energy conditions. Thanks to stable hysteresis during endurance cycles, repeated potentiation and depression were also mimicked without an ageing effect. To the best of our knowledge, this is the first presentation of a methodology for an ultra-low energy driven synaptic transistor. We expect that this research will pave the way for future research on ultra-low energy consuming synaptic transistors using other oxide semiconductor combinations or EDL materials, based on this strategy.

Experimental section

Fabrication of the synaptic transistors

The synaptic transistors proposed in this study have TGBC structures, as shown in Fig. 1a. First, ITO films were deposited on a glass substrate, patterned, and used as S/D electrodes. Subsequently, 30 nm of IGZO and 4 nm of IZO, which are the main layers of the devices, were deposited by RF sputtering at room temperature at a partial oxygen pressure of 30%. Before GI deposition, pre-annealing was conducted at 350 °C for 2 h under an oxygen atmosphere. An oxygen atmosphere was formed by injecting oxygen gas after vacuuming the inside of the furnace. Next, 10 nm of Al_2O_3 films were deposited using PEALD at 200 °C. Trimethyl aluminium ($(CH_3)_3Al$, TMA) and 60 W of oxygen plasma were used as precursors of Al and oxygen, respectively. After Al_2O_3 film deposition, a 30 nm-thick SiO_2 EDL was deposited by PEALD at 200 °C. In this step, BDEAS ($H_2Si[N(C_2H_5)_2]_2$) and 100 W of oxygen plasma were used as Si and oxygen reactants, respectively. Finally, 75 nm-thick Mo films, for use as the gate electrodes, were deposited by DC sputtering. All the layers were patterned by conventional photolithography and wet etching processes, allowing the synaptic transistors to have a relatively small physical size.[1] The width and length of the active layers of the synaptic transistors were 40 and 20 μm, respectively.

Electrical measurements and characterizations

The electrical characteristics of the neuromorphic transistors were measured under ambient conditions (25 °C, humidity 50%) in the dark probe station, using HP4284A, HP4156A, HP41501A and Keithley 4200A-SCS. Seven samples were fabricated and measured to confirm the uniformity and deviation. The thickness of the thin films was measured using a spectroscopy ellipsometer (ALPHA-SE). The constituent elements of the thin films were analysed by performing SIMS (IMS7f). The bonding states were analysed by FT-IR spectroscopy (IFS66V/S). To calculate the density of thin films, XRR (SmartLab) was conducted. The XPS depth profile (K-alpha) was obtained to determine the atom distribution and bonding state based on the thickness of the double oxide semiconductors. The carrier concentrations of the oxide semiconductors were obtained using Hall measurement (HL5500PC). Finally, an image of the fabricated device and deposited thin films was obtained through UC-EF-TEM (Libra 200 MC TEM).

Conflicts of interest

There are no conflicts to declare.

Acknowledgements

This work was supported by Samsung Display Corporation through KAIST Samsung Display Research Centre Program. This work was also supported by a National Research Foundation of Korea (NRF) grant funded by the Korea government (MSIT) (2018R1A2A3075518 and 2020M3F3A2A0108191611).

Notes and references

1 S. L. Dai, Y. W. Zhao, Y. Wang, J. Y. Zhang, L. Fang, S. Jin, Y. L. Shao and J. Huang, *Adv. Funct. Mater.*, 2019, **29**, 1903700.
2 D. Kuzum, S. M. Yu and H. S. P. Wong, *Nanotechnology*, 2013, **24**, 382001.
3 J. Jiang, J. J. Guo, X. Wan, Y. Yang, H. P. Xie, D. M. Niu, J. L. Yang, J. He, Y. L. Gao and Q. Wan, *Small*, 2017, **13**, 1700933.
4 V. M. Ho, J. A. Lee and K. C. Martin, *Science*, 2011, **334**, 623–628.
5 J. J. Harris, R. Jolivet and D. Attwell, *Neuron*, 2012, **75**, 762–777.
6 D. Fioravante and W. G. Regehr, *Curr. Opin. Neurobiol.*, 2011, **21**, 269–274.
7 S. G. Kim, J. S. Han, H. Kim, S. Y. Kim and H. W. Jang, *Adv. Mater. Technol.*, 2018, **3**, 1800457.
8 K. M. Kim, J. M. Zhang, C. Graves, J. J. Yang, B. J. Choi, C. S. Hwang, Z. Y. Li and R. S. Williams, *Nano Lett.*, 2016, **16**, 6724–6732.
9 Y. B. Li, Z. R. Wang, R. Midya, Q. F. Xia and J. J. Yang, *J. Phys. D: Appl. Phys.*, 2018, **51**, 503002.
10 S. Y. Wang, D. W. Zhang and P. Zhou, *Sci. Bull.*, 2019, **64**, 1056–1066.
11 M. Suri, V. Sousa, L. Perniola, D. Vuillaume and B. DeSalvo, 2011 International Joint Conference on Neural Networks (Ijcnn), 2011, 619–624.
12 E. Carlos, R. Branquinho, R. Martins, A. Kiazadeh and E. Fortunato, *Adv. Mater.*, 2021, **33**, 2004328.
13 Y. L. He, Y. Yang, S. Nie, R. Liu and Q. Wan, *J. Mater. Chem. C*, 2018, **6**, 5336–5352.
14 H. F. Ling, D. A. Koutsouras, S. Kazemzadeh, Y. van de Burgt, F. Yan and P. Gkoupidenis, *Appl. Phys. Rev.*, 2020, **7**, 011307.
15 M. K. Kim and J. S. Lee, *Nano Lett.*, 2019, **19**, 2044–2050.
16 Q. T. Wu, J. W. Wang, J. C. Cao, C. Y. Lu, G. H. Yang, X. W. Shi, X. C. Chuai, Y. X. Gong, Y. Su, Y. Zhao, N. D. Lu, D. Geng, H. Wang, L. Li and M. Liu, *Adv. Electron. Mater.*, 2018, **4**, 1800556.

17 J. Kim, Y. Kim, O. Kwon, T. Kim, S. Oh, S. Jin, W. Park, J. D. Kwon, S. W. Hong, C. S. Lee, H. Y. Ryu, S. Hong, J. Kim, T. Y. Heo and B. Cho, *Adv. Electron. Mater.*, 2020, **6**, 1901072.
18 M. K. Park, H. N. Yoo, Y. T. Seo, S. Y. Woo, J. H. Bae, B. G. Park and J. H. Lee, *ACS Appl. Electron. Mater.*, 2020, **2**, 323–328.
19 J. Jiang, W. N. Hu, D. D. Xie, J. L. Yang, J. He, Y. L. Gao and Q. Wan, *Nanoscale*, 2019, **11**, 1360–1369.
20 R. Martins, P. Barquinha, L. Pereira, N. Correia, G. Goncalves, I. Ferreira and E. Fortunato, *Appl. Phys. Lett.*, 2008, **93**, 203501.
21 Z. Ye, Y. G. Yuan, H. Xu, Y. Liu, J. K. Luo and M. Wong, *IEEE Trans. Electron Devices*, 2017, **64**, 438–446.
22 R. Martins, P. Barquinha, L. Pereira, N. Correia, G. Goncalves, I. Ferreira and E. Fortunato, *Phys. Status Solidi RRL*, 2009, **3**, 308–310.
23 G. D. Feng, J. Jiang, Y. H. Zhao, S. T. Wang, B. Liu, K. Yin, D. M. Niu, X. H. Li, Y. Q. Chen, H. G. Duan, J. L. Yang, J. He, Y. L. Gao and Q. Wan, *Adv. Mater.*, 2020, **32**, 1906171.
24 J. M. Zhou, N. Liu, L. Q. Zhu, Y. Shi and Q. Wan, *IEEE Electron Device Lett.*, 2015, **36**, 198–200.
25 C. J. Wan, L. Q. Zhu, Y. H. Liu, P. Feng, Z. P. Liu, H. L. Cao, P. Xiao, Y. Shi and Q. Wan, *Adv. Mater.*, 2016, **28**, 3557–3563.
26 J. Li, Y. H. Yang, Q. Chen, W. Q. Zhu and J. H. Zhang, *J. Mater. Chem. C*, 2020, **8**, 4065–4072.
27 D. P. Liu, Q. Q. Shi, S. L. Dai and J. Huang, *Small*, 2020, **16**, 1907472.
28 C. Zhang, S. Y. Wang, X. L. Zhao, Y. H. Yang, Y. H. Tong, M. X. Zhang, Q. X. Tang and Y. C. Liu, Adv. Funct. Mater., 2020, DOI: ARTN 2007894. 10.1002/adfm.202007894.
29 Y. Liu, X. W. Wang, W. J. Chen, L. Y. Zhao, W. Zhang, W. J. Cheng, Z. T. Zhuo, J. Wang, T. L. Ren and J. Xu, *Superlattices Microstruct.*, 2019, **128**, 177–180.
30 L. Q. Guo, H. Han, L. Q. Zhu, Y. B. Guo, F. Yu, Z. Y. Ren, H. Xiao, Z. Y. Ge and J. N. Ding, *ACS Appl. Electron. Mater.*, 2019, **11**, 28352–28358.
31 T. Kamiya, K. Nomura and H. Hosono, *J. Disp. Technol.*, 2009, **5**, 273–288.
32 E. Fortunato, P. Barquinha and R. Martins, *Adv. Mater.*, 2012, **24**, 2945–2986.
33 T. Kamiya and H. Hosono, *NPG Asia Mater.*, 2010, **2**, 15–22.
34 M. Lorenz, M. S. R. Rao, T. Venkatesan, E. Fortunato, P. Barquinha, R. Branquinho, D. Salgueiro, R. Martins, E. Carlos, A. Liu, F. K. Shan, M. Grundmann, H. Boschker, J. Mukherjee, M. Priyadarshini, N. DasGupta, D. J. Rogers, F. H. Teherani, E. V. Sandana, P. Bove, K. Rietwyk, A. Zaban, A. Veziridis, A. Weidenkaff, M. Muralidhar, M. Murakami, S. Abel, J. Fompeyrine, J. Zuniga-Perez, R. Ramesh, N. A. Spaldin, S. Ostanin, V. Borisov, I. Mertig, V. Lazenka, G. Srinivasan, W. Prellier, M. Uchida, M. Kawasaki, R. Pentcheva, P. Gegenwart, F. M. Granozio, J. Fontcuberta and N. Pryds, *J. Phys. D: Appl. Phys.*, 2016, **49**, 433001.
35 J. Rosa, A. Kiazadeh, L. Santos, J. Deuermeier, R. Martins, H. L. Gomes and E. Fortunato, *ACS Omega*, 2017, **2**, 8366–8372.
36 G. J. Jeon, S. H. Lee, S. H. Lee, J. B. Shim, J. H. Ra, K. W. Park, H. I. Yeom, Y. Nam, O. K. Kwon and S. H. K. Park, *Sci. Rep.-Uk*, 2019, **9**, 3216.
37 P. Feng, W. W. Xu, Y. Yang, X. Wan, Y. Shi, Q. Wan, J. W. Zhao and Z. Cui, *Adv. Funct. Mater.*, 2017, **27**, 1604447.
38 K. Kim, C. L. Chen, Q. Truong, A. M. Shen and Y. Chen, *Adv. Mater.*, 2013, **25**, 1693–1698.
39 C. S. Yang, D. S. Shang, N. Liu, G. Shi, X. Shen, R. C. Yu, Y. Q. Li and Y. Sun, *Adv. Mater.*, 2017, **29**, 1700906.
40 A. M. Shen, K. Kim, A. Tudor, D. Lee and Y. Chen, *Small*, 2015, **11**, 1571–1579.
41 J. T. Yang, C. Ge, J. Y. Du, H. Y. Huang, M. He, C. Wang, H. B. Lu, G. Z. Yang and K. J. Jin, *Adv. Mater.*, 2018, **30**, 1801548.
42 P. F. Carcia, R. S. McLean, M. H. Reilly, M. K. Crawford, E. N. Blanchard, A. Z. Kattamis and S. Wagner, *J. Appl. Phys.*, 2007, **102**, 074512.
43 J. S. Park, J. K. Jeong, Y. G. Mo, H. D. Kim and C. J. Kim, *Appl. Phys. Lett.*, 2008, **93**, 033513.
44 J. B. Wang, Y. X. Li, Y. Yang and T. L. Ren, *IEEE Electron Device Lett.*, 2017, **38**, 588–591.
45 Y. Kim, K. H. Lee, G. Mun, K. Park and S. H. K. Park, *Phys. Status Solidi A*, 2017, **214**, 1700183.
46 D. Gaspar, J. Martins, P. Bahubalindruni, L. Pereira, E. Fortunato and R. Martins, *Adv. Electron. Mater.*, 2018, **4**, 1800423.
47 J. H. Cho, J. Lee, Y. He, B. Kim, T. P. Lodge and C. D. Frisbie, *Adv. Mater.*, 2008, **20**, 686–690.
48 M. J. Panzer and C. D. Frisbie, *Adv. Mater.*, 2008, **20**, 3177–3180.
49 J. Sun, Q. Wan, A. X. Lu and J. Jiang, *Appl. Phys. Lett.*, 2009, **95**, 222108.
50 L. A. Kong, J. Sun, C. Qian, G. Y. Gou, Y. K. He, J. L. Yang and Y. L. Gao, *Org. Electron.*, 2016, **39**, 64–70.
51 J. Jiang, Q. Wan, J. Sun and A. X. Lu, *Appl. Phys. Lett.*, 2009, **95**, 152114.
52 S. G. Jeong, H. J. Jeong, W. H. Choi, K. Kim and J. S. Park, *IEEE Trans. Electron Devices*, 2020, **67**, 4250–4255.
53 K. D. Kreuer, *Chem. Mater.*, 1996, **8**, 610–641.
54 H. W. Du, X. Lin, Z. M. Xu and D. W. Chu, *J. Mater. Sci.*, 2015, **50**, 5641–5673.
55 J. B. Ko, S. H. Lee, K. W. Park and S. H. K. Park, *RSC Adv.*, 2019, **9**, 36293–36300.
56 K. Ide, K. Nomura, H. Hosono and T. Kamiya, *Phys. Status Solidi A*, 2019, **216**, 1800372.
57 C. J. Wan, J. M. Zhou, Y. Shi and Q. Wan, *IEEE Electron Device Lett.*, 2014, **35**, 414–416.
58 Y. Kang, B. Du Ahn, J. H. Song, Y. G. Mo, H. H. Nahm, S. Han and J. K. Jeong, *Adv. Electron. Mater.*, 2015, **1**, 1400006.
59 S. H. K. Park, M. K. Ryu, H. Oh, C. S. Hwang, J. H. Jeon and S. M. Yoon, *J. Vac. Sci. Technol., B*, 2013, **31**, 020601.
60 H. K. Noh, K. J. Chang, B. Ryu and W. J. Lee, *Phys. Rev. B: Condens. Matter Mater. Phys.*, 2011, **84**, 115205.
61 E. H. P. Cordfunke, R. J. M. Konings and W. Ouweltjes, *J. Chem. Thermodyn.*, 1991, **23**, 451–454.
62 G. D. Wu, P. Feng, X. Wan, L. Q. Zhu, Y. Shi and Q. Wan, *Sci. Rep.-Uk*, 2016, **6**, 23578.

63 L. Q. Zhu, C. J. Wan, L. Q. Guo, Y. Shi and Q. Wan, *Nat. Commun.*, 2014, **5**, 3158.
64 X. Wan, Y. Yang, P. Feng, Y. Shi and Q. Wan, *IEEE Electron Device Lett.*, 2016, **37**, 299–302.
65 C. J. Wan, L. Q. Zhu, J. M. Zhou, Y. Shi and Q. Wan, *Nanoscale*, 2013, **5**, 10194–10199.
66 C. G. Van de Walle, *Phys. Rev. Lett.*, 2000, **85**, 1012–1015.
67 D. M. Hofmann, A. Hofstaetter, F. Leiter, H. J. Zhou, F. Henecker, B. K. Meyer, S. B. Orlinskii, J. Schmidt and P. G. Baranov, *Phys. Rev. Lett.*, 2002, **88**, 045504.
68 Y. H. Liu, L. Q. Zhu, P. Feng, Y. Shi and Q. Wan, *Adv. Mater.*, 2015, **27**, 5599–5604.
69 W. Xu, S. Y. Min, H. Hwang and T. W. Lee, *Sci. Adv.*, 2016, **2**, e1501326.