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Atomic layer deposition-enabled trench oxide thin-film transistors with selective dry etching for high-current driving applications

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ABSTRACT

Trench-structured thin-film transistors (TFTs) based on oxide semiconductors have attracted increasing attention for next-generation high-resolution displays, owing to their compact footprint and potential for high current-driving capability in short-channel configurations. However, prior approaches to increasing the current in trench-structured oxide TFTs often rely on non-uniform thicknesses induced by sputtering, which are difficult to control and reproduce. This paper presents a trench TFT with an oxide semiconductor active layer deposited via atomic layer deposition (ALD) combined with selective protective layer (PL) dry etching. The optimized device with a short channel length of 5.51 μm achieves an ultra-high normalized on-current of 163.2 μA/μm and on/off ratio exceeding 10^{10} at a drain voltage of 4.1 V. Directional dry etching selectively removes the PL from the horizontal device regions, significantly altering their electrical properties while preserving the integrity of the vertical channel. This enables region-specific electrical tuning that overcomes the uncontrolled characteristics of conventional trench TFTs formed by non-uniform deposition. Multiple characterization techniques confirmed that BCl_3 dry etching introduces shallow donor-like states near the etched surface, effectively increasing the free-carrier concentration in the horizontal channel regions. This localized doping lowers the channel resistance, and thereby contributes to a significant improvement in the overall electrical performance. The optimized ALD-based trench TFT exhibits a favorable subthreshold swing (0.108 V/dec) and acceptable turn-on voltage (−0.68 V). These results demonstrate that the ALD trench TFT with selective dry etching provides a promising strategy for future high-performance ultra-high-resolution display backplanes

1. Introduction

Oxide semiconductor thin-film transistors (TFTs) have been promising candidates for next-generation displays because of their advantages such as high mobility exceeding 100 $cm^2/V\cdot s$ [1,2], superior flexibility, uniformity, and stability [2,3]. The energy-efficient operation enabled by their low leakage current makes them suitable candidates for mobile and wearable applications. Despite these advantages, the application of oxide TFTs in ultra-high-resolution displays remains challenging. This is because the number of scan lines in the backplane increases with an increase in the display resolution, which reduces the line scan time (time per line) and consequently shortens the pixel charging time, thereby leading to insufficient signal strength. Further, the reduced pixel size of high-resolution displays constrains the available area of each TFT. Thus, TFTs that can overcome these limitations are required to maintain display performance. To address this issue, oxide TFTs must have high mobility to deliver sufficient current despite reduced charging times. A high on-current is crucial for enhancing average brightness and ensuring the effective integration of devices and circuits. Although oxide TFTs are widely used in large-area active-matrix organic light-emitting diode panels, their relatively low mobility and on-current prevent them from replacing low-temperature polysilicon TFTs in high-resolution mobile devices.

Consequently, considerable research has focused on enhancing the driving currents of oxide TFTs. For example, Lee et al. enhanced the mobility and current of indium-gallium oxide TFTs by introducing a tantalum (Ta) capping layer, which catalyzed low-temperature crystallization at 200–250 °C [4]. The Ta layer promotes oxygen diffusion because of its low Gibbs free energy, weakened metal–oxygen bonds, and induced lattice ordering near the interface, which results in

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improved mobility and device stability. Chen et al. [5] showed that double-gate indium-gallium-zinc oxide TFTs enhance mobility and driving current by concentrating electron transport in the central channel region, which has fewer hydrogen-related traps than the top and bottom interfaces. However, these approaches do not address the deterioration of electrical properties associated with device miniaturization. The drain current decreases proportionally with the narrowing of the channel width [6], and shorter channel lengths can cause the contact resistance to become more dominant than the channel resistance, further reducing charge mobility [7,8]. In addition, short-channel oxide TFTs often suffer from negative threshold voltage (V_{th}) shifts, which pose further design challenges. Vertical oxide TFTs have been explored for achieving high on-currents in compact layouts [9–11]. However, their fabrication involves complex processes that introduce issues such as voids and shadowing, which degrade their electrical performance. Dry etching, which is commonly used to define vertical structures, further contributes to defect formation on the spacer surface, negatively affecting the subthreshold swing (SS).

In our previous study, we developed a trench TFT that demonstrated high on-current despite a small footprint [12]. In this trench TFT, the horizontally thick regions of the active layer function as highly conductive current paths, whereas the vertically thin regions serve as effective channels, which result in an on-current boosting effect. The fabrication process was straightforward and compatible with conventional planar TFT technology, yielding a reasonable turn-on voltage (V_{on}) and good SS. However, the active layer was deposited via sputtering, which led to a non-uniform thickness on the trench sidewall because of the inherent anisotropy of the process and equipment geometry. Such thickness variations depend on specific tool configurations and are difficult to control. Therefore, a more systematic approach is required to ensure reproducibility and design flexibility.

The need for smaller, more reliable, and high-performance TFTs in display backplanes has become increasingly critical as display technology advances toward higher resolutions. Short-channel TFTs are susceptible to variations in the uniformity of the active layer, which directly influences the device performance and stability. Atomic layer deposition (ALD), with its self-limiting growth mechanism, enables precise thickness control, superior film uniformity, and excellent conformality, even in complex device structures [13,14]. In addition, ALD affords a fine-tuned material composition by adjusting the number of precursor cycles, thereby enabling optimized electrical properties [14,15]. The low-temperature processing compatibility of this process makes it suitable for flexible and next-generation displays [13,16]. Further, ALD provides high repeatability and scalability for large-area manufacturing, thereby ensuring process reliability [13]. Given these advantages, ALD is considered essential for realizing high-performance, stable, and uniform TFTs for future display technologies.

In this paper, we propose an ALD-based trench TFT (denoted as AT-TFT) incorporating a conformal oxide semiconductor active layer to overcome the limitations of conventional sputtering processes used in trench TFT fabrication and satisfy the requirements of next-generation display technologies. In our previous study on sputter-based trench TFTs, the high on-current was attributed to differences in the electrical properties between the horizontal and vertical sections, which arose from variations in the active-layer thickness caused by the limited step coverage of sputtering [12]. However, conformal deposition by ALD could not replicate this thickness variation. To overcome this, we introduced selective protective layer (PL) dry etching to induce electrical property differences between the horizontal and vertical sections. The PL is extensively removed from the horizontal regions because of the directional nature of dry etching, which significantly alters its electrical properties. In contrast, the vertical sections undergo minimal PL dry etching, preserving the active layer and reducing the susceptibility to etching-induced effects. This selective process induces distinct electrical characteristics across different regions of the TFT and facilitates the on-current-boosting effect.

The AT-TFT demonstrated an exceptionally high normalized on-current of 163.2 μA/μm at a drain voltage (V_{DS}) of 4.1 V, along with a low off-current in the range of 10^{-13} A, which resulted in an on/off ratio exceeding 10^{10}. Further, the device exhibited a favorable SS of 0.108 V/dec and reasonable V_{on} of −0.68 V. Moreover, we elucidate the operating mechanism and superior electrical performance of the AT-TFT formed through selective dry etching of PL, highlighting its significant potential for next-generation electronic devices such as the semiconductor devices, displays, and sensors.

The remainder of this paper describes the fabrication of the proposed AT-TFT and details the electrical characterization that reveals the impact of selective dry etching on the device performance. It then discusses the underlying mechanisms contributing to the current enhancement, including the effects of doping and geometry, and concludes with the implications of this approach for future high-resolution display technologies.

2. Experimental

2.1. Fabrication of AT-TFT

Fig. 1 illustrates the schematic structure of the ALD-based planar and trench TFTs (denoted as AP-TFT and AT-TFT, respectively) and the fabrication process of the AT-TFT. The AP-TFT was fabricated on the same substrate as the AT-TFT following an identical fabrication process, except for the trench hole formation step.

To fabricate the AT-TFT, a 255-nm-deep trench hole was initially created on a thermal SiO_2 (T-SiO_2) layer via reactive-ion etching. Subsequently, a ~150-nm-thick indium tin oxide layer was sputtered as the source/drain electrodes, followed by vacuum annealing at 250 °C for 2 h and patterning using photolithography and wet etching. Next, a ~10-nm-thick indium zinc oxide (IZO) film was deposited at 200 °C via plasma-enhanced ALD (PEALD), followed by photolithography and wet etching. [3-(Dimethylamino)propyl]dimethyl indium and diethylzinc were utilized as indium and zinc precursors, respectively, and 100 W O_2 plasma was used as the oxygen reactant. A ~10-nm-thick aluminum oxide (Al_2O_3) PL was deposited by PEALD using trimethylaluminum and O_2 plasma at 60 W and 200 °C, followed by vacuum pre-annealing at 280 °C for 2 h. The PLs were then dry-etched with BCl_3 and Ar gas for 0, 5, 10, 15, and 20 s. Dry etching was performed under the following conditions: BCl_3 and Ar at 50 sccm each, RF power of 500 W, chamber pressure of 30 mTorr, and substrate temperature of 25 °C. An additional ~25-nm-thick Al_2O_3 layer was deposited as the gate insulator under the same conditions as those used for the PL. Furthermore, a ~150-nm-thick molybdenum (Mo) gate electrode was deposited via sputtering and patterned via photolithography and wet etching. Finally, a post-annealing was performed at 150 °C under vacuum for 30 min.

An AT-TFT subjected to 15 s of PL dry etching was selected as the optimized device. The fabricated AT-TFT device had channel dimensions of approximately 20 μm (width) and 5.51 μm (length), which included a 5 μm horizontal channel and two 0.255 μm vertical channels. Although the AP-TFT shares the same channel dimensions as the AT-TFT from the top view (approximately 20 μm width and 5 μm length), the actual channel length differs due to the absence of the vertical section.

2.2. Characterization

The electrical characteristics of the devices were measured using an HP 4156 A semiconductor parameter analyzer (Agilent). The transfer and output curves were obtained under ambient conditions. Transmission electron microscopy (TEM), secondary ion mass spectrometry (SIMS), X-ray photoelectron spectroscopy (XPS), and Hall effect measurements were performed to investigate the effects of dry etching on the device performance.

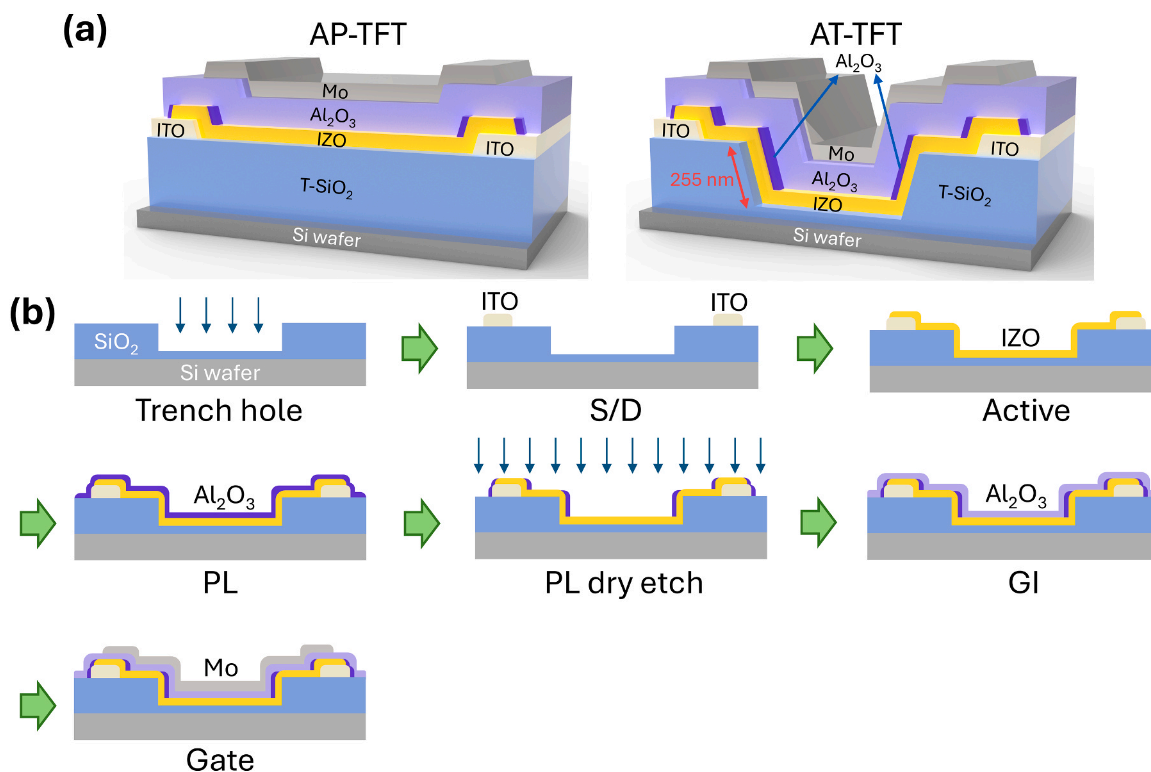

Fig. 1. (a) Schematic of the AP- and AT-TFTs, showing a vertical channel length of 255 nm on one side of the AT-TFT, and (b) Fabrication process of the AT-TFT.

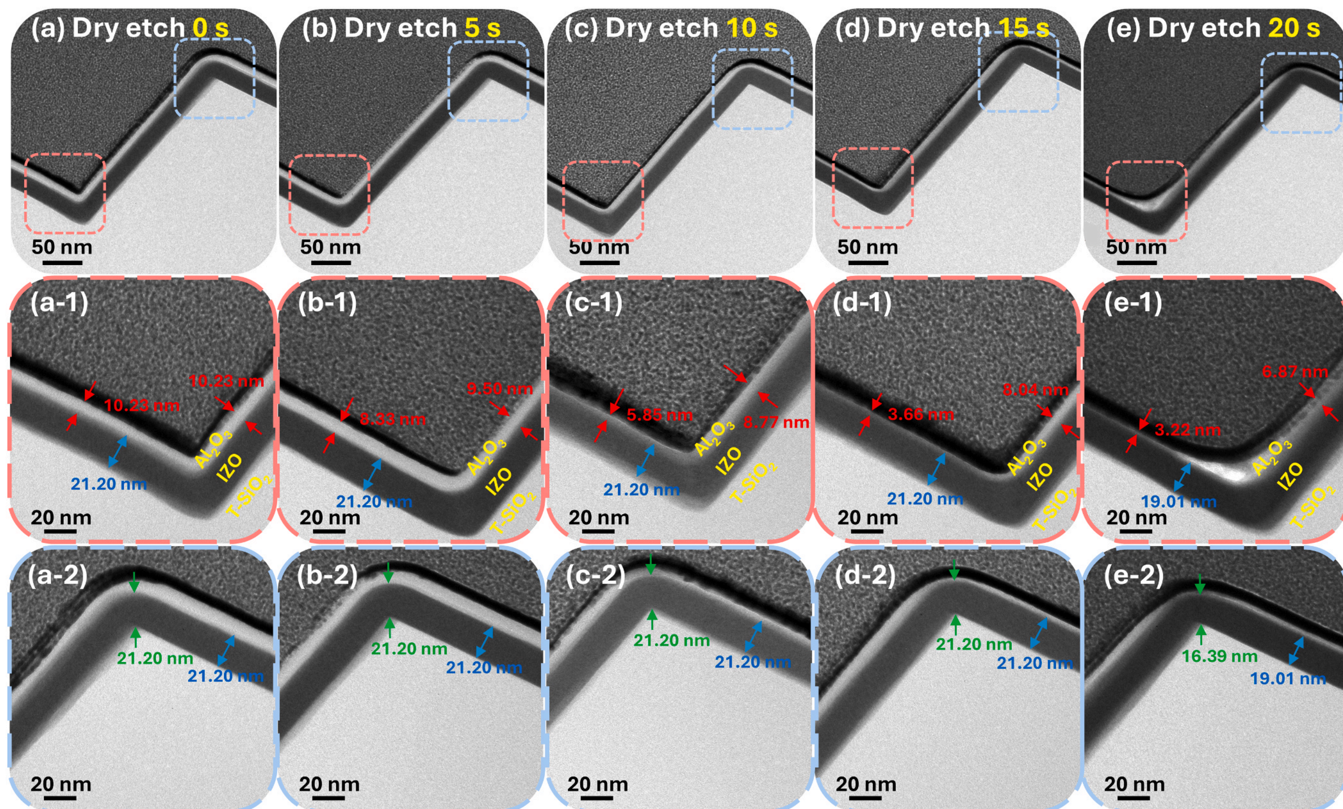

Fig. 2. Cross-sectional TEM images of Al_2O_3 PLs subjected to dry etching for various durations: (a) 0 s, (b) 5 s, (c) 10 s, (d) 15 s, and (e) 20 s. Blue numbers: horizontal active layer thickness; green: convex corner active layer thickness; red: PL thickness.

3. Results and discussion

The directional nature of the dry etch gas during the dry etching of the Al_2O_3 PL retained only the PL in the vertical sidewall, while the horizontal surfaces were etched away. To investigate this phenomenon, a dry etch test was conducted on 10.23 nm of Al_2O_3 PL deposited on the 21.20-nm-thick IZO film deposited on a trench-structured T-SiO_2. Fig. 2 shows the TEM images from this test. The initial structure without etching (dry etching for 0 s), indicates that the Al_2O_3 PL was deposited conformally by ALD, thereby resulting in identical thicknesses on both the horizontal and vertical surfaces (10.23 nm each). As the etching time increased, the anisotropic nature of the dry etching process led to a preferential thinning of the horizontal regions. The Al_2O_3 thicknesses for the horizontal and vertical surfaces were measured as follows: 0 s, 10.23 nm / 10.23 nm; 5 s, 8.33 nm / 9.50 nm; 10 s, 5.85 nm / 8.77 nm; 15 s, 3.66 nm / 8.04 nm; and 20 s, 3.22 nm / 6.87 nm. Although the PL in the horizontal region was completely removed for 15 s and longer, cross-sectional TEM still revealed an apparent ultrathin layer (~3 nm). This contrast is attributed not to residual PL, but to the horizontal redeposition of etch by-products after complete PL removal [17–19]. Fig. 3 summarizes the amount of Al_2O_3 PL removed by dry etching in the horizontal and vertical regions over time, as extracted from the TEM measurements. The etching rate on the horizontal region (0.44 nm/s) was ~2.75 times higher than that on the vertical region (0.16 nm/s). The etching rate was extracted from the slope of the linearly fitted curve of the removed PL thickness as a function of dry-etch time. For the horizontal region, the 20 s data point was excluded from the fitting because the PL was fully etched only after 15 s, and the ~3 nm layer observed thereafter was attributed to redeposition rather than residual PL. This vertical/horizontal selective etching creates differences in TFT characteristics between the vertical and horizontal regions.

AT-TFTs with different PL dry etching times were fabricated to investigate the impact of dry etching on the TFT characteristics, and Fig. 4(a) displays their transfer curves measured at $V_{DS} = 0.1$ V. Further, AP-TFTs were fabricated on the same substrate as the AT-TFTs to facilitate easier characterization of the AT-TFT. These AP-TFTs are identical to AT-TFTs in all aspects, except for the absence of the trench hole; therefore, they can reasonably approximate the electrical characteristics of the horizontal region in the AT-TFTs. Furthermore, the electrical characteristics of the AP-TFT without PL dry etching (0 s) can be used as a reference to infer the properties of the vertical regions of the AT-TFTs because they are mostly protected by PL and are minimally affected by dry etching.

As shown in Fig. 4(a), AP-TFTs with PL etching times of 0 and 5 s exhibited on/off properties, indicating a relatively high resistance. Based on our previous study on trench TFTs, they can be conceptualized as a series connection of planar-vertical-planar-vertical-planar TFTs (Fig. 4(b)) [12]. Therefore, AT-TFTs with PL etching times of 0 and 5 s included a series of connections of TFTs exhibiting distinct on/off characteristics, which resulted in moderate on-current on/off performances.

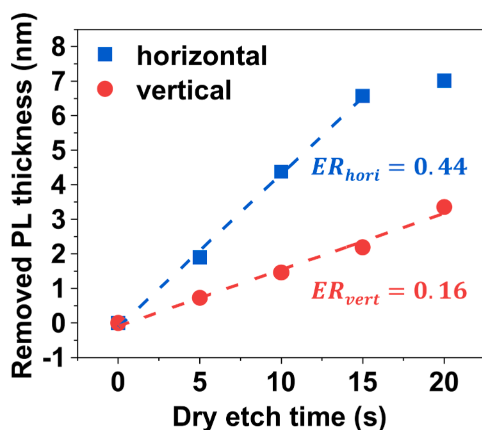

Fig. 3. Measured thickness of the PL removed by dry etching as a function of etch time.

However, AP-TFTs with PL etching times of 10 and 15 s exhibited conductor-like behaviors across the entire gate voltage (V_G) range, which suggests that AT-TFTs with etch times of 10 and 15 s are composed of vertical TFTs with on/off properties and planar TFTs with conductive properties. Because the vertical and horizontal regions function as effective channels and current pathways, respectively, AT-TFTs with etching times of 10 and 15 s exhibit significantly enhanced on/off current ratios and pronounced current-boosting effects. The on/off current ratio was improved by factors of ~685 and 8581 compared to that of the AT-TFT without dry etching.

In the case of 20 s, the AP-TFT exhibited conductive behavior across the entire V_G range while showing an approximately one-order reduction in the on-current compared to the 10 and 15 s cases. This degradation in current level is attributed to multiple factors:

(1) Over-etching, which reduces the IZO thickness, as shown in Fig. 2 (e-1) and (e-2). The thickness remains ~21.20 nm up to 15 s of dry etching; however, it decreases to 19.01 nm after 20 s, indicating damage to the active layer. This contributes to an increased channel resistance because oxide semiconductors show a reduction in the total number of carriers with decreasing thickness, yielding a positive shift in the transfer curve and a reduced on-current [20–23].
(2) The presence of ionized dopant atoms reduces the current increase owing to carrier scattering.

However, these two mechanisms cannot entirely explain why the 20 s AT-TFT exhibits an even lower on-current than that of the 5 s case. This discrepancy can be further understood by examining the etched profile near the convex trench step, as shown in Figs. 2(a-2)–(e-2). Although the IZO thickness at this corner remained constant (~21.20 nm up to 15 s), it was significantly reduced to 16.39 nm at 20 s, representing a decrease of 22.7 %. This value is 13.8 % lower than that of the horizontal region (19.01 nm), which has already undergone partial erosion because of the complete removal of the Al_2O_3 PL and subsequent damage to the underlying IZO layer. The corner region experienced even more severe thinning, which indicates that etching at the convex step was further accelerated beyond that of the flat horizontal surfaces. This excessive thinning is attributed to the broadened ion incidence angles at the convex corners resulting in a locally intensified ion flux, and the electric field distortion at the convex geometries (the tip shape effect) enhancing the local ion flux [24–26]. Together, these effects accelerate etching at the corners, leading to excessive material removal. In addition, over-etching at the convex corner generated noticeable surface roughness on the IZO surface, which was more clearly observed in the TEM image of the completed TFT (Fig. S1). This roughness increases carrier scattering, reduces the mean free time, and consequently suppresses both mobility and current. The resulting thinning of the active layer at the corner, combined with the increased surface roughness owing to over-etching, introduces a bottleneck in the current flow in the vertical transition region. This accounts for the lower on-current observed in the 20 s AT-TFT compared to that in the 5 s case, despite a more conductive horizontal region. The 15 s etching condition was selected as an optimized parameter that offers the highest on/off current ratio, smallest hysteresis, and reasonable V_{on}.

The observed on-current boosting effect induced by dry etching is primarily attributed to elemental doping by BCl_3 gas. Chlorine (Cl), a Group 17 element similar to fluorine (F), has been recognized for its role as a shallow donor in oxide semiconductors by substituting the oxygen sites [27–30]. Similarly, low-level boron (B) doping in zinc oxide increases carrier concentration, reduces resistivity, and improves mobility

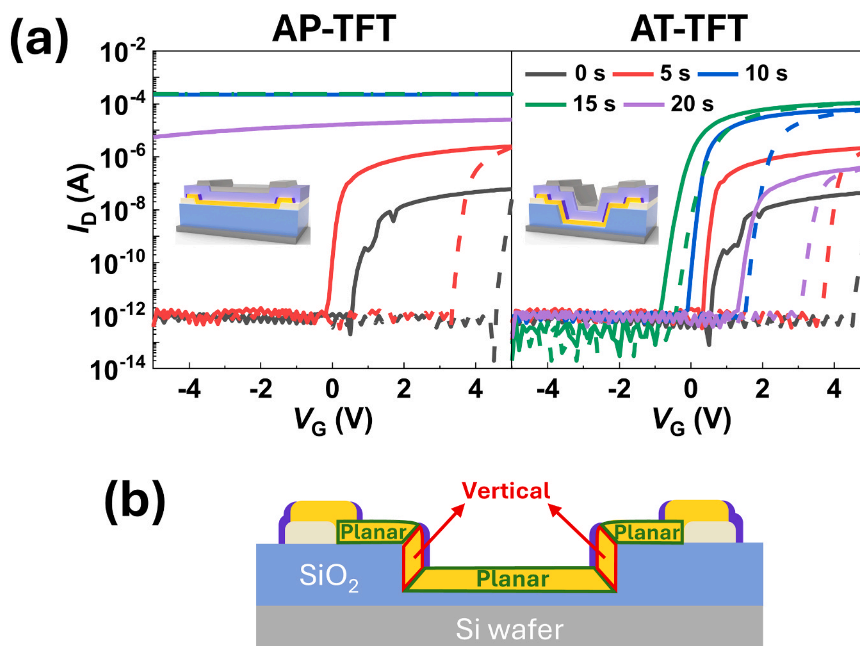

Fig. 4. (a) Transfer characteristics of AP-TFTs and AT-TFTs fabricated with varying PL dry etch times (0, 5, 10, 15, and 20 s), measured at $V_{DS} = 0.1$ V. Solid lines represent the forward sweep and dashed lines indicate the backward sweep. (b) Conceptual representation of the AT-TFT structure as a series connection of planar and vertical TFT segments. For clarity of illustration, the GI and gate electrode are omitted here.

by substituting Zn^{2+} cations with B^{3+} cations [31–33].

To clarify this mechanism, Fig. 5 illustrates the band diagrams of the vertical and horizontal channel regions of the AT-TFT. In the PL-retained vertical region, dopant incorporation is minimal, keeping the Fermi level lower and preserving the switching characteristics. In contrast, in the horizontal channel region, Cl and B substitutions create shallow donor states located only a few tens of meV below the conduction band minimum (CBM). Electrons in these states are readily excited into the conduction band, shifting the Fermi level closer to the CBM, thereby markedly increasing the free-electron concentration and reducing channel resistance.

Fig. 6 presents the SIMS and XPS results used to analyze the doping impact of BCl_3 dry etching on IZO according to the etching time, and Fig. S2 shows the sample preparation process. Fig. 6(a) shows the SIMS data of Cl and B and Fig. 6(b) shows the mean intensity of these elements in the front channel (diagonally hatched areas in Fig. 6(a)), where the actual channel is formed. The results indicate that the Cl and B concentrations increase with extended dry etching time, with Cl exhibiting a particularly significant increase at 20 s. A similar tendency is also observed in the XPS data. In Fig. 6(c), the XPS peak intensity of Cl is not distinctly observed at 0, 5, and 10 s, whereas a small peak appears at 15 s, followed by a significant increase at 20 s. The XPS peak intensity of B is noticeable at 15 s, with a slight increase at 20 s. At 0, 5, and 10 s, the absence of Cl and B peaks can be attributed to their concentrations being below the detection limit.

In the case of the Zn $2p_{3/2}$ XPS data, a gradual positive shift was observed with increasing dry etch time, shifting from 1020.92 eV at 0 s to 1021.40 eV at 20 s. This positive shift reflects a modification of the local chemical environment of Zn, and is consistent with an increasing fraction of Zn–Cl bonds [30]. The incorporation of Cl at the O sites, in

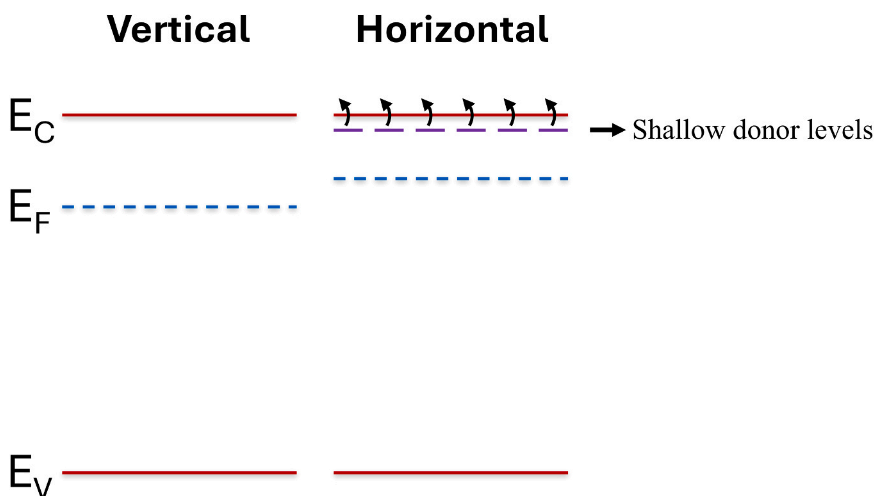

Fig. 5. Band diagrams of the vertical and horizontal channel regions of the AT-TFT. In the vertical channel, limited doping keeps the Fermi level remains farther from the CBM, resulting in lower carrier concentration and stronger gate control. In contrast, Cl and B shallow-donor states introduced by BCl_3 dry etching in the horizontal channel donate electrons to the conduction band, shifting the Fermi level closer to the CBM, thereby increasing free electron density and reducing channel resistance.

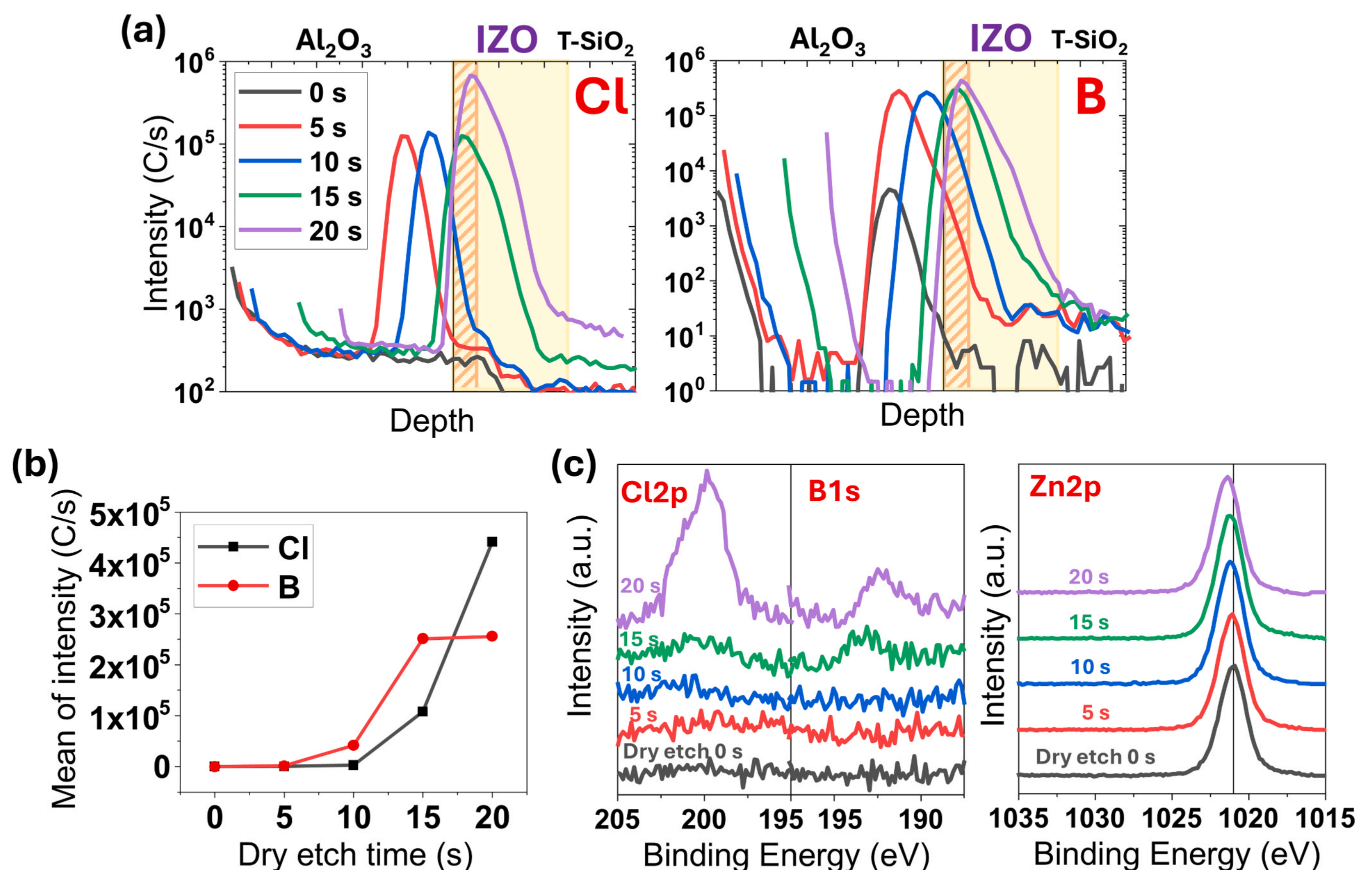

Fig. 6. (a) SIMS depth profiles of Cl and B in Al_2O_3/IZO/T-SiO_2 stack films subjected to BCl_3 dry etching with varying etch times. (b) Mean intensities of Cl and B extracted from the front-channel region (diagonally hatched area in (a)). (c) XPS peak intensities of Cl2p, B1s, and Zn2p by varying PL dry etching time.

turn, may influence the local electronic structure and contribute to donor-like behavior.

The Hall measurement analysis results are presented in Table 1, and the sample fabrication process is shown in Fig. S3. For the 0, 5, and 10 s samples, measurements were not possible because of the high resistance. For the 20 s dry etching sample, the carrier concentration increased to 2.19×10^{20} cm^{-3} compared to that of the 15 s sample (1.70×10^{20}); in addition, the resistivity decreased from 1.573×10^{-3} Ω·cm to 1.278×10^{-3} Ω·cm. This further confirmed that Cl and B doping effectively increased the free carrier concentration. Despite the increase in carrier concentration, the Hall mobility decreased from 23.4 cm^2/V·s to 22.3 cm^2/V·s. This reduction in mobility can be attributed to the high Cl doping level, which induces scattering by ionized dopant atoms, thereby limiting electron transport [27]. Along with the reduced IZO thickness, the scattering by ionized dopant atoms results in lower on-currents in AP- and AT-TFTs with 20 s of dry etching compared to those with 15 s (Fig. 4).

Although these analyses were conducted using horizontal test structures, the results are highly relevant to vertical regions. When the PL thickness remains comparable, horizontal data can serve as a reliable approximation of vertical sidewall behavior. Furthermore, excess dopants incorporated into the horizontal regions are likely to diffuse toward the adjacent vertical corners, thereby increasing the carrier concentration in those areas. As a result, the effective channel length may become shorter than the purely geometric vertical dimension, leading to a significant enhancement of the overall on-current.

Table 1
Hall measurement results of IZO films after BCl_3 dry etching with different etch times. Electrical parameters were only measurable for etch times of 15 s and 20 s due to high resistance at lower etch durations.

Etch time	Resistivity (Ω·cm)	Mobility (cm^2/V·s)	Bulk Conc (cm^{-3})
15 s	1.573×10^{-3}	23.4	-1.70×10^{20}
20 s	1.278×10^{-3}	22.3	-2.19×10^{20}

Fig. 7(a) shows the transfer characteristics of AP- and AT-TFTs with a PL dry-etching time of 15 s under various V_{DS} conditions. The AP- and AT-TFT curves for 15 s shown in Fig. 4(a), correspond to those measured at $V_{DS} = 0.1$ V. The AT-TFT with a 15 s etching time was selected as the optimal device because of its highest on/off current ratio, minimal hysteresis, and reasonable V_{on} among devices etched for 0–20 s. The horizontal section of the AT-TFT was inferred to be similarly conductive because the AP-TFT exhibited conductor-like behavior across the entire V_G sweep. Meanwhile, the vertical sections, which were less affected by dry etching, functioned as effective high resistance channels that determined the on/off characteristics. The device achieved a high on-current while maintaining a reasonable V_{on} value because these vertical and horizontal sections were connected in series. Along with the reduction of the effective channel length to the submicron scale by B and Cl doping, dopant diffusion from the horizontal regions into the vertical corners further shortened the effective channel length below the vertical dimension, thereby producing an exceptionally high on-current. Fig. 7 (b) shows the output curves of the AT-TFT with a PL dry etching time of 15 s; the curves demonstrate good saturation behavior with an increase in V_{DS}.

Fig. 8(a) presents the transfer curves at $V_{DS} = 0.1$ V for a conventional TFT (C-TFT), and the optimized AT-TFT fabricated in this study. The C-TFT refers to a planar device with a ~10 nm IZO active layer fabricated without the PL dry etching process (serving as a reference for performance comparison and distinct from the AP-TFT). Fig. 8(b) presents a comparison of the key parameters of the devices. The SS was calculated using

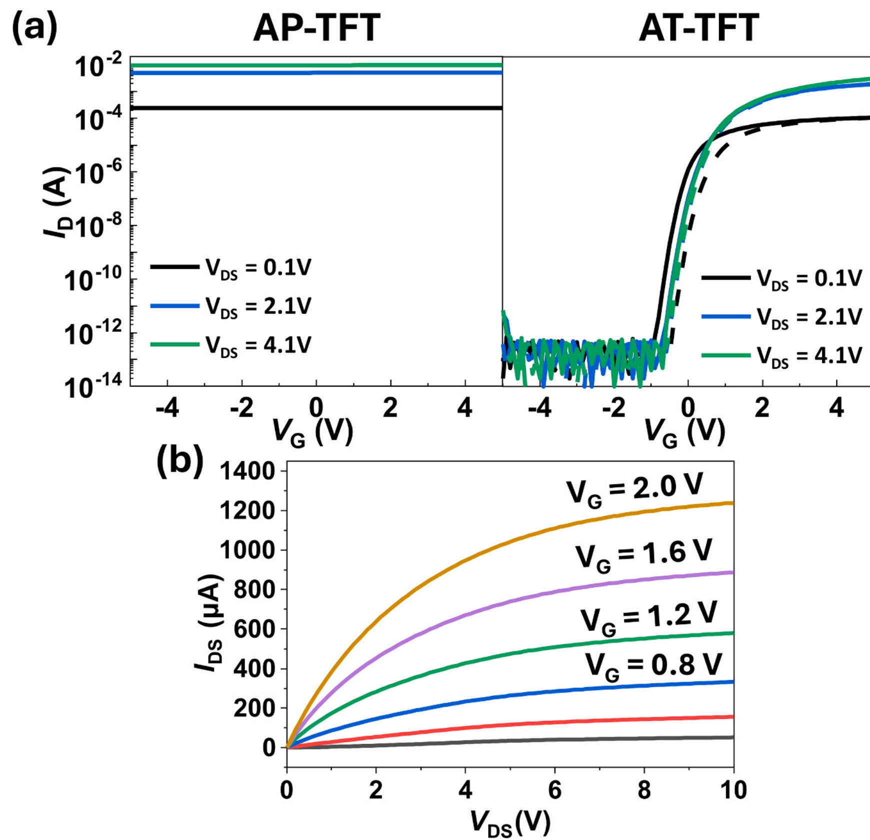

Fig. 7. (a) Transfer characteristics of AP-TFT and AT-TFT with a PL dry etching time of 15 s. Solid lines represent the forward sweep and dashed lines indicate the backward sweep. (b) Output characteristics of the optimized AT-TFT, showing well-saturated drain current behavior with increasing V_{DS}.

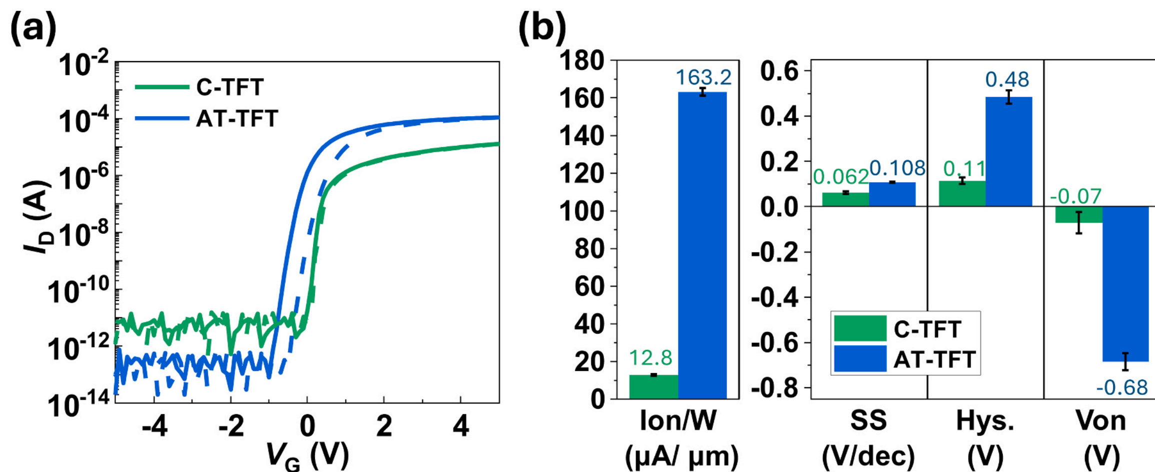

Fig. 8. (a) Transfer characteristics of the C-TFT, and the optimized AT-TFT developed in this study, measured at $V_{DS} = 0.1$ V. Solid lines represent the forward sweep, while dashed lines indicate the backward sweep. (b) Comparison of key electrical parameters, including normalized on-current (I_{on}/W), SS, hysteresis, and V_{on}.

$$SS = \frac{dV_G}{d(\log I_D)}, \quad (1)$$

where I_D represents the drain current. V_{on} was selected as V_G at a I_D of $10pA \times (W/L)$.

The optimized AT-TFT exhibits a remarkably high normalized on-current of 163.2 μA/μm at $V_{DS} = 4.1$ V, which is ~12.8 times higher than that of the C-TFT of 12.8 μA/μm. Furthermore, the device achieved an ultra-high on/off current ratio exceeding 10^{10}. In addition, the device exhibited a favorable SS of 0.108 V/dec, which was slightly higher than that of the C-TFT (0.062 V/dec). The higher current driving of AT-TFT led to a negative shift in V_{on}, from −0.07 V in the C-TFT to −0.68 V in the AT-TFT. Further, the hysteresis increased to 0.48 V because of defect generation from the PL dry etching process relative to 0.11 V in the C-TFT. Although this hysteresis can be mitigated by carefully controlling the PL dry-etching time to minimize direct damage to the IZO active layer, this presents a trade-off between stability and performance, as the etching time also directly determines the extent of BCl_3-derived doping and, thus, the on-current. Furthermore, the trench sidewall roughness, which is transferred from the photoresist during anisotropic dry etching when forming the trench hole, aggravates hysteresis by disturbing the carrier transport along the vertical channel. Although not yet

implemented in this study, we expect that introducing a mild wet etching step after trench formation could reduce the sidewall roughness and significantly mitigate hysteresis in the vertical channel region.

The optimized device exhibited comparable V_{on} shifts of 1.6 V to the C-TFT of 1.7 V under positive-bias temperature stress (PBTS) after 10,000 s at an electric field of 1 MV/cm and 60 °C (Supporting Information, Fig. S4). Over the same stress, the linear mobility changed only slightly both for the C-TFT (from 32.1 to 32.3 $cm^2/V \cdot s$, +0.6 %), and for the AT-TFT (from 516.9 to 521.6 $cm^2/V \cdot s$, +0.9 %). The SS showed a small increase in the C-TFT (0.072 → 0.073 V/dec, +1.4 %), but a decrease in the AT-TFT (0.116 → 0.109 V/dec, −6.0 %). As shown in Fig. S5, the AT-TFT exhibits a negative temperature coefficient of V_{on} shift (higher T → smaller shift), consistent with rapid de-trapping from shallow states which suppresses V_{on} shift. However, etch-induced damage can introduce additional traps that degrade stability; the balance of these competing effects yields a V_{on} shift close to that of the C-TFT and suggests a dielectric-limited asymptote common to both stacks. Because the AT-TFT stability arises from coupled, competing mechanisms, a definitive mechanistic assignment is beyond the scope of this work and will be pursued as a separate follow-up study. The long-term reliability (weeks–months) will likewise be assessed under thermal aging and environmental exposure.

The reproducibility of the fabricated devices was also evaluated. For the C-TFT, the standard deviation (SD) of the linear mobility was 1.58 $cm^2/V \cdot s$, while for the AT-TFT it increased to 50.97 $cm^2/V \cdot s$. Similarly, the normalized on-current exhibited SD values of 1.04 μA/μm and 7.23 μA/μm for the C-TFT and AT-TFT, respectively. This higher variability in the AT-TFT is attributed to the substantial carrier concentration enhancement induced by BCl_3 doping, which amplifies the sensitivity of device characteristics to fluctuations in doping level. In addition, non-uniformities in the dry-etching process may introduce position-dependent variations in the effective doping concentration across the substrate. As a result, the mobility and on-current can differ markedly among devices, fabricated under nominally identical conditions, leading to reduced reproducibility of the BCl_3-doped AT-TFT compared to the C-TFT.

Table 2 summarizes the key characteristics and parameters of previously reported oxide TFTs with trench structures. Compared to these devices, the AT-TFT presented in this work exhibited a slightly larger hysteresis and a more negative V_{on}. However, it operated reliably even at a shorter channel length (~5.51 μm) and demonstrated significantly higher mobility (505.5 $cm^2/V \cdot s$) and normalized on-current (163.2 μA/μm) than those of the other trench TFTs, which typically show mobility values of approximately 100 $cm^2/V \cdot s$. The linear mobility value (μ_{lin}) was calculated as

$$\mu_{lin} = \frac{g_m}{\left(\frac{W}{L}\right) \bullet C_{ox} \bullet V_{DS}}, \tag{2}$$

where g_m and C_{ox} represent the transconductance and the capacitance of the GI, respectively. Collectively, these results highlight the strong potential of the proposed AT-TFT for next-generation ultra-high-resolution display and semiconductor applications.

Although the AT-TFT structure includes a highly conductive horizontal path and a vertical effective channel (conditions that can result in an overestimation of field-effect mobility), we present the extracted mobility value (505.5 $cm^2/V \cdot s$) for benchmarking purposes. This decision is justified by the fact that previously reported trench TFT studies, which feature similar current-path configurations and share the same potential for mobility inflation, have reported mobility values without reservation [34–36].

In addition to these trench TFT precedents, several studies on metal-capping-layer TFTs, which exhibit significant current boosting through alternative current paths, have reported high mobility values, even when structural or doping-related factors affect the measurement. For example, the work by Kim et al. explicitly uses the term "apparent field-effect mobility" to acknowledge that mobility enhancement may not solely reflect intrinsic transport but rather series resistance reduction and interface effects [37]. Choi et al. reported high mobility; however, through the concept of a "supplement source" provided by the capping layer, they suggested that the mobility may be structurally inflated rather than reflecting intrinsic channel behavior [38].

Previous studies on trench TFTs with separate horizontal conduction and vertical channel regions, as well as on metal capping TFTs with auxiliary conduction layers, have demonstrated that mobility values are commonly reported, even when structural effects may cause overestimation. In this context, the inclusion of mobility in our study ensured a fair and direct comparison with previous studies. However, we emphasize the normalized on-current for a more accurate assessment of device performance.

4. Conclusions

In this study, we fabricated and validated a novel AT-TFT utilizing selective PL dry etching to address the limitations of conventional trench TFTs. By employing ALD rather than sputtering for the active layer, superior conformality and uniformity were achieved in the trench structure, which is expected to further enhance scalability. The optimized device achieved a remarkably high normalized on-current of 163.2 μA/μm and on/off ratio of $> 10^{10}$ at a drain voltage of 4.1 V, surpassing previous oxide trench TFT designs. This exceptional performance is attributed to the distinct electrical characteristics in the vertical and horizontal device regions resulting from selective directional dry etching and BCl_3-induced doping effects. In addition, the optimized AT-TFT exhibited a favorable SS of 0.108 V/dec, reasonable V_{on} of −0.68 V, compatibility with large-area fabrication, and straightforward integration with conventional TFT technologies. However, the observed hysteresis and negative shift in V_{on} indicate that further optimization of the etching and doping processes is necessary. Future studies will focus on further improvements in device stability, hysteresis reduction, and

Table 2
Summary of key parameters of previously reported oxide TFTs with trench structures, compared with the proposed AT-TFT.

Ref.	Process	Channel material	Ion/W (μA/μm)	μ_{lin} ($cm^2/V \cdot s$)	SS (V/dec)	Hys (V)	V_{on} (V)	TFT W, L (μm)
[12]	sputtering	Al:ITZO†	27.7 (V_{DS} = 4.1 V)	69	0.122	0.3	−0.4	20, 5.46
[34]	sputtering	Al:ITZO	0.745 (V_{DS} = 0.1 V)	98.19	-	negligible	−0.5	20, 10.4
[35]	PEALD	IO‡	-	129	-	0	−0.4	20, 10.4
[36]	PEALD	IZO	9.86 (V_{DS} = 4.1 V)	87.85	0.073	~0	~0	20, 10
This work	PEALD	IZO	163.2 (V_{DS} = 4.1 V)	505.5	0.108	0.48	−0.68	20, 5.51

†Al:ITZO = Aluminum–doped indium–tin–zinc–oxide
‡IO = Indium oxide

mitigation of negative V_{on} shifts through optimized doping conditions, defect management, and advanced passivation techniques, which can enable the practical implementation of AT-TFTs in next-generation display systems. Additionally, the integration of this architecture with flexible or transparent substrates, as well as its scalability to submicron geometries, represents a promising direction for high-resolution and next-generation display backplanes.

CRediT authorship contribution statement

Do Hyung Kim: Writing – review & editing, Writing – original draft, Visualization, Validation, Supervision, Project administration, Methodology, Investigation, Formal analysis, Conceptualization. **Hyunjun An:** Conceptualization. **Jong Beom Ko:** Writing – review & editing. **Sang-Hee Ko Park:** Writing – review & editing, Supervision, Resources, Project administration, Funding acquisition.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper

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Appendix A. Supporting information

Supplementary data associated with this article can be found in the online version at doi:10.1016/j.jallcom.2025.184565.

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Glossary List

ALD: Atomic layer deposition
AT-TFT: ALD-based trench TFT
C-TFT: Conventional TFT
IZO: Indium zinc oxide
PEALD: Plasma-enhanced ALD
PL: Protective layer
SIMS: Secondary ion mass spectrometry
SS: Subthreshold swing

TEM: Transmission electron microscopy
TFTs: Thin-film transistors
XPS: X-ray photoelectron spectroscopy