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Outstanding Performance as Cu Top Gate IGZO TFT With Large Trans-Conductance Coefficient by Adopting Double-Layered Al_2O_3/SiN_x Gate Insulator

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Gate insulator (GI) materials in top gate structured InGaZnO thin-film transistor (TFT) with copper gate electrode are examined for the application to the large area display. To overcome the problems with hydrogen diffusion, which can influence the number of carriers in oxide semiconductor and to gain large trans-conductance coefficient, a double-layered GI of 30 nm Al_2O_3/ 120 nm SiN_x is adopted. The TFT showed field-effect mobility, V_{on}, *SS*, and hysteresis of 12.8 $cm^2 V^{-1} s^{-1}$, −0.7 V, 0.17 V $decade^{-1}$, and almost 0 V, respectively, and the ΔV_{on} under the positive bias stress of 20 V and negative bias stress of −20 V at 60 °C for 10 000 s are +0.1 and −0.4 V, respectively.

1. Introduction

To realize ultra-high resolution display in large size, oxide thin film transistor (TFT) is expected to be the best among other TFT candidates such as a-Si TFT, Low Temperature Poly Silicon (LTPS) TFT, and MoS_2 TFT.[1,2] In spite of several disadvantages like sensitivity to the process and materials, instability originated from the defects related to the hydrogen and oxygen, and negative V_{th} shift in TFT with short channel length less than 2 um,[3] it is considered to have advantages such as low off current and scalability.[4–6] Especially materialization of diverse device structures with good performance makes oxide TFT possible to be applied to drive Liquid Crystal Display (LCD) and Organic Light Emitting Diode (OLED) without any limitation in display size. Among the TFT structures, top gated self-aligned (SA) TFT is considered as the most suitable structure for the large sized high resolution active matrix OLED due to the decreasing RC delay from smallest parasitic capacitance, and increasing I_{ds} current from high trans-conductance coefficient *K*, defined as ($\mu_{eff} \times C_{ox}$), where μ_{eff} is a field effective mobility and C_{ox} is the capacitance of gate insulator (GI).[7,8]

To obtain large trans-conductance coefficient of TFT in practical technology, it is necessary to adopt relatively high-k dielectric materials such as SiN_x.[1,9,10] In case of top gate oxide TFT, however, it is very difficult to deposit SiN_x film directly on top of the active layer in the form of single layer or even double layers of SiO_x/SiN_x owing to the H incorporation into the active layer during the film deposition, inducing V_{th} negative shift of TFT.[10–13] Furthermore, deposition of GI even SiO_2 by plasma-enhanced chemical vapor deposition (PECVD) in top gate structure is limited in applying high temperature deposition or high temperature heat treatment after deposition of GI because of the difficulty in controlling the number of carriers in oxide semiconductor. This process temperature limitation results in worse stability of top gate (TG) oxide TFT under positive bias temperature stress (PBTS) and negative bias temperature stress (NBTS).[14]

Here, we examined the effect of GI in a TG IGZO TFT, mimicking a SA structure to investigate the capability of inhibiting H diffusion into the active layer as well as the high current driving ability. We applied thin Al_2O_3 film deposited by atomic layer deposition (ALD) as a first GI to suppress diffusion of extra hydrogen into the channel area during the deposition process and post treatment in order to form high-performance insulator with no generation of plasma damage on top of the active layer.[5,15] As a second GI, SiO_x, and SiN_x deposited by PECVD were adopted in consideration of its dielectric constant and degree of H incorporation into the active layer during the deposition process.[16–17] We analyzed film characteristics and properties of each transistor with the different stack of GI to compare the effect of each dielectric. In the case of applying Al_2O_3 deposited by thermal ALD at 300 °C as the first dielectric GI forming interface with active layer, excellent characteristics of the transistors with even SiN_x as the 2nd bulk GI were verified.

2. Experimental

The staggered typed TG Indium Gallium-Zinc-Oxide (1:1:1 atomic ratio, IGZO) TFT has been fabricated. TG structured TFT can represent interface states between oxide semiconductor and

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DOI: 10.1002/pssa.201700183

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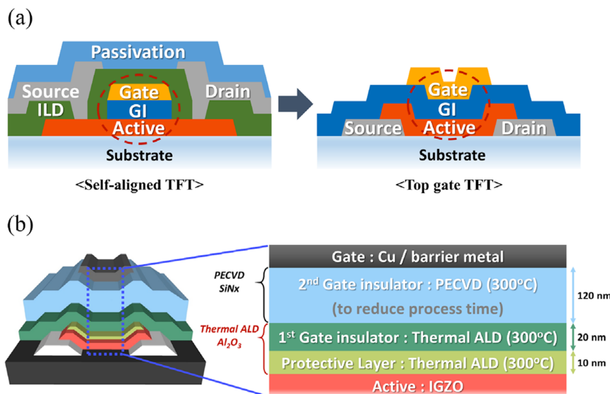

Figure 1. (a) Schematic diagram of self-aligned TFT and top gate TFT shows that sequences of stacked layers of active/GI/gate are the same, and (b) cross-section of top gate structured IGZO TFT fabricated with double layered GI and Cu gate.

GI, and GI and metal gate by mimicking SA structured TFT (**Figure 1**(a)). First, we manufactured IGZO TFT with molybdenum (Mo) gate and various GI layers applied in order to investigate TFT properties depending on GIs. The detailed process for the fabrication of TFT was previously reported as shown in Figure 1.[18] After simultaneous patterning of the IGZO layer with active protection layer (PL), we deposited three kinds of main GIs on each sample, as follows: (a) 140 nm Al_2O_3 by ALD at 300 °C (device A) using TMA and water as precursors, (b) a double layer of 20 nm Al_2O_3 by thermal ALD at 300 °C/120 nm SiO_2 by PECVD at 300 °C, (device B) and (c) a double layer of 20 nm Al_2O_3 by thermal ALD at 300 °C/120 nm SiN_x by PECVD at 300 °C (device C). Here, the PL protects the surface of active layer from the contamination during the photolithography and the chemical damage during the active etching process.[18]

For the second experiment, we applied Cu and IGZO with 1:1:2.5 atomic ratio film, showing higher mobility than that of 1:1:1 IGZO TFT as a gate electrode and active layer, respectively, to the device A and C considering application to the large area display. We inserted Mo barrier layer to improve adhesion of Cu and GI. The thickness of the each metal layer was 10 and 100 nm for Mo and Cu, respectively. All the samples fabricated were post-annealed under vacuum at 300 °C for 2 h. Also, samples of stacked layers without patterning were simultaneously deposited sequentially in the same way as for the transistors to analyze the thin film composition.

The transfer characteristics of the transistors with the size of width and length of 40 and 20 um respectively, were measured at 0.1 and 10 V of drain voltage. The field-effect mobility (μ_{FE}) was extracted in the linear region using following equation:

$$\mu_{FE} = L g_m / W C_i V_{ds}. \tag{1}$$

where W and L are the channel width and length, respectively. The V_{on} was defined as V_g when I_{ds} is $(W/L) \times 10^{-12}$ A. The stacked films were used for the measurement of secondary ion mass spectroscopy (SIMS) to analyze the degrees of incorporation or diffusion of H and Cu into the IGZO active layer. The dielectric constant of each single film and stacked films are calculated from the C–V data and film thickness of the device of

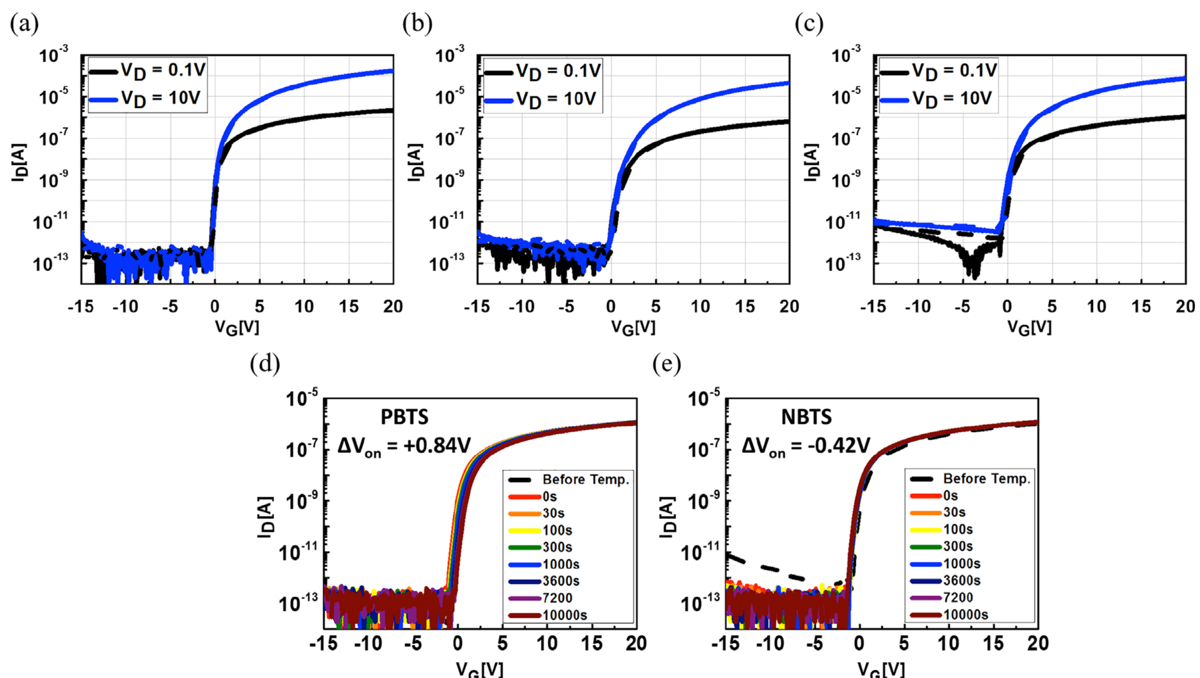

Figure 2. Transfer curve of the annealed top gate structured TFTs with Mo gate and GI of (a) Al_2O_3 by thermal ALD only (TFT A), (b) Al_2O_3 by thermal ALD/SiO_2 by PECVD (TFT B), and (c) Al_2O_3 by thermal ALD/SiN_x by PECVD (TFT C). Transfer curve of the TFT C during (d) PBTS and (e) NBTS stress of gate bias 20 and −20 V, respectively at 60 °C.

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metal/insulator/metal which was fabricated with TFT at the same time.

3. Results and Discussion

We fabricated TG transistor with double-layered GI, Al_2O_3/SiN_x, of high-k dielectric, which doesn't cause diffusion of hydrogen into the active layer, has no defect, and performs as a good Cu barrier as well. Although thermal ALD process of Al_2O_3 using H_2O precursor does not cause any plasma damage at the interface, it induces hydrogen (H) incorporation or diffusion into the active during the deposition or thermal annealing, respectively, depending on the process temperature as does PECVD SiO_2 or SiN_x process. The main difference between the ALD Al_2O_3 film and PECVD processed films is that Al_2O_3 itself has H barrier properties. Therefore, suppressing both H incorporation during the just initial deposition of Al_2O_3 and diffusion of H from initially deposited thin Al_2O_3 into the active layer during the thermal annealing is necessary. We set the Al_2O_3 deposition temperature at 300 °C to minimize the H diffusion during the thermal annealing. Since ALD process takes time to deposit thick GI, the practical method in designing the GI with high dielectric constant and H barrier ability is an adoption of double GI with thin ALD processed GI and thick PECVD processed GI.

Figure 2 shows the transfer characteristics of TFTs with three different GIs and identical Mo gate. Transistors with GI composed of double-layered, Al_2O_3/SiO_2 (TFT B) and Al_2O_3/SiN_x (TFT C), were compared to those with only Al_2O_3 (TFT A), in terms of mobility, V_{on}, and sub-threshold swing (SS). The TFT A (Figure 2(a)) post annealed at 300 °C showed field-effect mobility, V_{on}, SS, and hysteresis of 9.71 $cm^2 V^{-1} s^{-1}$, −0.3 V, 0.16 V $decade^{-1}$, and 0.1 V, respectively. Meanwhile, TFT B showed the properties of 7.08 $cm^2 V^{-1} s^{-1}$, 0.12 V, 0.36 V $decade^{-1}$, and 0.1 V, respectively (Figure 2(b)). Figure 2(c) is the transfer curve of TFT C; the values were 8.46 $cm^2 V^{-1} s^{-1}$, −0.58 V, 0.27 V $decade^{-1}$ and 0.1 V, respectively.

In spite of forming the same interfaces between the active and the first GI of thin Al_2O_3, the 2nd GI process influenced the interface trap density ($D_{it,max}$) of each TFT. The $D_{it,max}$ of TFT A, B, and C, extracted from the equation of SS showed 4.827×10^{11}, 9.259×10^{11}, and 4.397×10^{11} $cm^{-2} eV^{-1}$, respectively by applying different dielectric constant values of each GI.[12,19] Dielectric

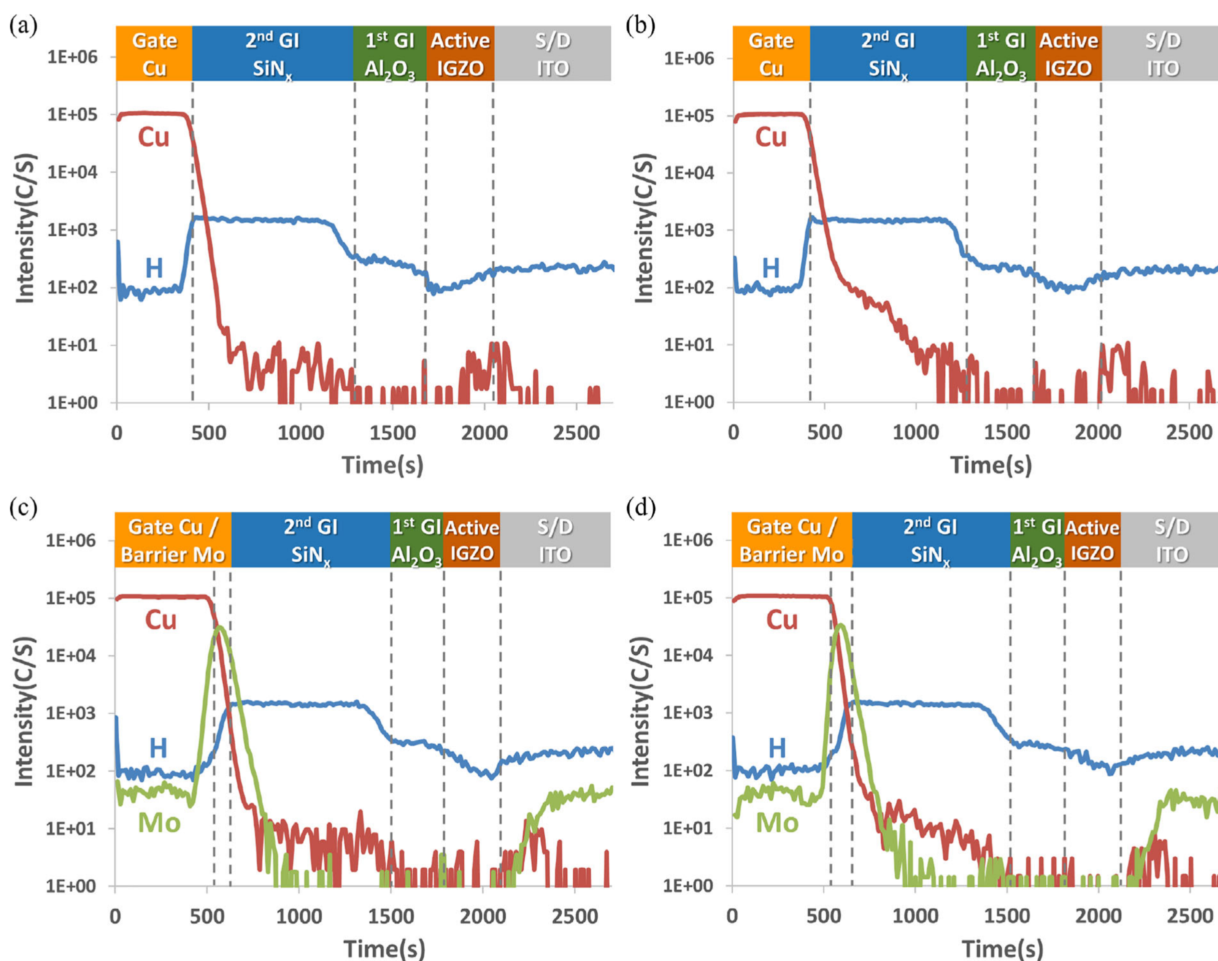

Figure 3. SIMS result of Cu, H, and Mo amount in the sample without Mo barrier (a) before and (b) after annealing at 300 °C under vacuum, and with Mo barrier (c) before and (d) after annealing.

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constant values for TFT A, B, and C are 7.6, 4.9, and 6.3, respectively. In the second GI process, SiN_x by PECVD induces less generation of interface trap density even than by ALD process of Al_2O_3. We assume that it is because the small amounts of H incorporated into the interface during the SiN_x process passivate the defects in the interface between the active and GI. The largest negative value of V_{on} of TFT C among three TFTs can also be ascribed to the increased carrier amounts by hydrogen incorporation during the SiN_x process.

This kind of beneficial effect of H diffusion from the GI into the active layer has been reported.[20] However, too much of hydrogen diffusion rather results in huge negative V_{on} shift of oxide TFT, thus controlling of H amount in the active layer and interface between the active and GI is the key process to obtain well behaved oxide TFT.

Although only 30 nm Al_2O_3 did not function as GI to block H diffusion completely, it still acted as a good H barrier.[10,21] Most of TG IGZO TFTs adopted SiO_2 as a GI because direct SiN_x deposition or additional deposition on SiO_2 causes V_{on} shift negatively and higher I_{off}.[10,13,17,21] Our TG IGZO TFT with Al_2O_3/SiN_x, however, shows only −0.3 V difference to that of V_{on} of alumina only TFT even after being post-annealed at 300 °C. In terms of I_{ds} current, while the value of TFT with Al_2O_3/SiO_2 at V_{gs} of 20 V is 4.3×10^{-5} A, that of TFT with Al_2O_3/SiN_x shows 7.5×10^{-5} A. The use of high-k dielectric layer of SiN_x increased the on-current level almost twice without any dielectric leakage. The ΔV_{on} of TG IGZO TFT with Al_2O_3/SiN_x under the positive bias stress of 20 V and negative bias stress of −20 V at 60 °C for 10 000 s were +0.84 and −0.42 V, respectively (Figure 2(d) and (e)). Therefore, adoption of double GI of ALD Al_2O_3 and PECVD SiN_x in TG IGZO TFT yields not only high drain current but also high bias stability without causing any significant V_{on} negative shift thanks to the good interface formation with no plasma use of ALD process.

Numerous studies have been attempted to find the effect of low-resistance metal electrode Cu,[22,23] and the most serious issue is that Cu diffusion into GI or oxide active layer leads to severe degradation of electrical performance or reliability no matter which structure the transistor has.[16,24–27] Cu diffusion easily occurs under thermal or electrical stress, and the existence of Cu in GI, channel area, or interface induces trap density increasing.[17,24] Finally the induced traps result in degradation of mobility and SS, and increase of ΔV_{th}. Many studies have proved that Cu adopted devices showed V_{th} shift owing to charge trapping which is mainly due to Cu diffusion.[25] Additionally, it has been reported that Cu may be oxidized when forming interface with oxide at high temperature,[28] and that is one of the reasons we adopted SiN_x as a 2nd GI which is very well studied as an excellent Cu barrier. Furthermore, the high H barrier properties of ALD grown 1st GI of Al_2O_3 in TG IGZO TFT allow direct formation of SiN_x as the TFT passivation layer, which avoids oxidation of top surface of Cu gate electrode.[29,30]

Prior to manufacturing top gate transistors with Cu gate electrode, we analyzed film samples mimicking stacked layers of top gate structured TFT in order to verify whether Cu diffusion occurs or not. Without metal barrier between GI and Cu, **Figure 3**(a) and (b) show the SIMS data before (a) and after (b) post annealing at 300 °C under vacuum conditions. The layers of SIMS samples were stacked in the same sequence and thicknesses as those of transistors. A total of 30 nm-thick Al_2O_3

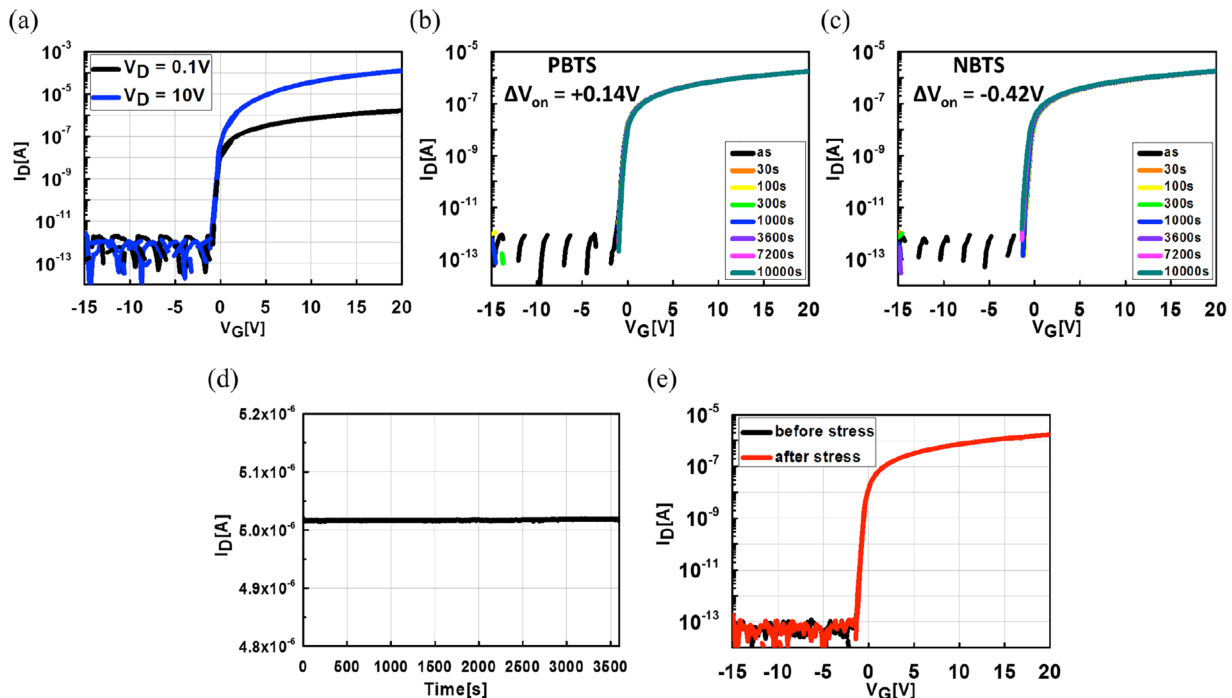

Figure 4. (a) Transfer curve of the top gate structured TFT with Mo/Cu gate annealed at 300 °C in vacuum for 2 h devices with double-layered GI of Al_2O_3/SiN_x, and its transfer curves during (b) PBTS and (c) NBTS stress of gate bias 20 and −20 V respectively at 60 °C (d) The amount of current flows during 3600 s at 3.85 V of gate voltage and 6.0 V of drain voltage. (e) Transfer curves before (black) and after (red) measurement of current stress.

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and 120 nm-thick SiN_x were used as a double-layered GI, and 80 nm-thick Cu gate metal was deposited. And the samples were also compared before(c) and after (d) post annealing at 300 °C in Figure 3(c) and (d) and they were applied with 10 nm-thick Mo as a barrier layer which improves adhesion of Cu and SiN_x. The results represent that SiN_x almost thoroughly prevents Cu diffusion regardless of annealing, despite the presence of tail states. Moreover, most importantly, Cu atoms do not exist in IGZO or interface with GI at all even after high temperature annealing process.

After verification that double-layered Al_2O_3/SiN_x definitely prevents bad influence of Cu electrode on electrical properties of oxide active layer, we manufactured top gate structured IGZO (1:1:2.5) TFT, showing higher mobility than that of 1:1:1 IGZO, and Cu top electrode. All the conditions were the same as for the previous top gate TFT with Mo gate electrode except additional Cu electrode. As we can see in **Figure** 4(a), field-effect mobility, V_{on}, SS, and hysteresis of the TFT are 12.8 $cm^2 V^{-1} s^{-1}$, −0.7 V, 0.17 V $decade^{-1}$, and almost 0 V, respectively. The ΔV_{on} under the positive bias stress of 20 V and negative bias stress of –20 V at 60 °C for 10 000 s were +0.1 and −0.4 V, respectively (Figure 4(b) and (c)). This result suggests that no additional trap was generated in channel area or interface between GI and channel.[6,31] If any more diffusion of Cu or hydrogen had occurred, not only stability degradation but also current decay by temperature and bias stress would have surely been observed.[25,26]

Since AMOLED is operated in current, it is necessary to verify the stability of currents under certain stress. We measured if there is any current changes at 3.85 V of gate voltage and 6.0 V of drain voltage which is the condition when about 5 uA of current flows, as shown in Figure 4(d) and (e). Figure 4(d) shows that there was almost no change in the amount of current for 3600 s. Figure 4(e) proves the result that not any shift happened after stress. With this result, we can say for sure that we fabricated competitive structured transistor to apply into large sized AMOLED.

4. Conclusions

We adopted double layered GI, thin 1st Al_2O_3, thick 2nd SiN_x GI, in TG IGZO TFT to firstly induce almost two fold increased I_{ds} current than that with SiO_2 at the designated V_{gs} and channel dimension without significant negative V_{th} shift and secondly to apply low-resistance Cu gate metal without causing Cu diffusion into the GI and active layer. TG structured IGZO (1:1:2.5) TFT with Cu gate has outstanding electrical properties with no bad influence either of thin 1st Al_2O_3, and thick 2nd GI of SiN_x, or of Cu metal. The IGZO (1:1:2.5 atomic ratio) TFT after post annealing at 300 °C under vacuum exhibited field-effect mobility, V_{on}, SS, and hysteresis of 12.8 $cm^2 V^{-1} s^{-1}$, −0.7 V, 0.17 V $decade^{-1}$, and almost 0 V, respectively. The ΔV_{on} under the positive bias stress of 20 V and negative bias stress of −20 V at 60 °C for 10 000 s were +0.1 and −0.4 V, respectively. It is suggested that applying double-layered GI including SiN_x can be adopted to manufacture highly reliable SA TFT with low-resistance electrode, Cu.

Acknowledgements

This research was funded by Samsung Display Corporation through KAIST Samsung Display Research Center Program and by Nano Material Technology Development Program through the National Research Foundation of Korea (NRF) funded by the Ministry of Science, ICT, and Future Planning (2016M3A7B4905609).

Conflict of Interest

The authors declare no conflict of interest.

Keywords

Al_2O_3/SiN_x GI, conductance coefficient, gate insulators, IGZO, TFT

Received: March 27, 2017
Revised: August 11, 2017
Published online: September 28, 2017

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