PAPER

Check for updates

Contact properties of a low-resistance aluminum-based electrode with metal capping layers in vertical oxide thin-film transistors†

Sori Jeon,[a] Kwang-Heum Lee,[a] Seung-Hee Lee, [ID][a] Seong-In Cho, [ID][a] Chi-Sun Hwang,[b] Jong Beom Ko [ID] *[a] and Sang-Hee Ko Park [ID] *[a]

Thin-film transistors (TFTs) with a small pitch size are necessary to realize high-resolution displays for virtual reality and augmented reality applications. Particularly, electrodes require low-resistance metals to reduce the resistance–capacitance delay caused by the increased pixel density. However, low-resistance Al can easily oxidize in bottom-contact structures of vertical TFTs owing to the oxidative deposition environment. This study quantitatively analyzed the contact properties of an Al-based metal with Mo and Ti capping layers. The Mo/Al/Mo and Ti/Al/Ti were adopted as the source/drain (S/D) electrodes, and their contact properties were compared. The top-gate bottom-contact device with Mo/Al/Mo S/D exhibited better contact properties, with a 0.02 V turn-on voltage (V_{on}), 3.5×10^7 ON/OFF ratio, and 5.7 kΩ contact resistance (R_{SD}). By contrast, the device with Ti/Al/Ti S/D exhibited degraded characteristics, with a -0.3 V V_{on}, 0.9×10^7 ON/OFF ratio, and 17 kΩ R_{SD} owing to metal oxidation. The contact properties were further examined through ultraviolet photoelectron spectroscopy, X-ray photoelectron spectroscopy, and transmission electron microscopy. Vertical TFTs were fabricated using Mo/Al/Mo and Ti/Al/Ti electrodes, and their electrical properties were investigated. The vertical TFT with Mo/Al/Mo electrodes exhibited reasonable performance, with a field-effect mobility of 3.3 cm^2 V^{-1} s^{-1} and R_{SD} of 15 kΩ. Conversely, the device with Ti/Al/Ti electrodes yielded degraded transfer characteristics, with a mobility of 0.05 cm^2 V^{-1} s^{-1} and R_{SD} of 984 kΩ. The analysis indicates that electrode materials significantly influence the electrical performance of vertical TFTs. Therefore, electrode materials must be carefully selected and structured to realize high-end vertical TFT arrays.

Introduction

Continuous development has significantly increased the number of Internet of Things[1] devices with enhanced connectivity. Therefore, next-generation displays with high-resolution, low-power consumption, and wearability are increasingly used as interfaces between devices.[2,3] Virtual reality (VR) and augmented reality (AR) displays require high-density pixels to present realistic images. To satisfy this demand, thin-film transistors (TFTs) with oxide semiconductors have been investigated owing to their advantages, such as adequate uniformity, high mobility, and low OFF-current.[4–6] High mobility oxide materials, such as indium–tin–zinc oxide (ITZO),[7] indium–zinc oxide (IZO),[8,9] indium–gallium–tin oxide (IGTO)[10] and indium oxide (In$_2$O$_3$),[11] have been actively researched to obtain high-performance TFTs. Additionally, gate insulators, such as HfO$_2$,[12] ZrO$_2$,[13] Al$_2$O$_3$,[14] and Al$_2$O$_3$/Si$_3$N$_4$ bi-layer[15] with high-k properties, are considered promising candidates for achieving high drain current.

The resistance of a metal electrode line is significant to the resistance–capacitance (RC) delay of high-resolution arrays. Therefore, low-resistance metals, such as copper (Cu)[16] and aluminum (Al),[17] are typically used for large area or high-resolution displays. Compared with Cu, Al does not exhibit metal diffusion issues and is inexpensive owing to its abundant availability.[18]

The electrode material determines the characteristics of oxide TFTs and RC delays. Previous studies have reported that TFT characteristics can significantly vary owing to channel shortening, metal diffusion, and contact resistance, which are associated with the electrode materials.[19,20] The contact resistance hinders the injection of charges from the source electrode, restricting current flow in the TFT despite using an excellent insulator and oxide semiconductor.

[a] Department of Materials Science and Engineering, KAIST, 291 Daehak-Ro, Yuseong-Gu, Daejeon 34141, Republic of Korea. E-mail: kojb914@kaist.ac.kr, shkp@kaist.ac.kr

[b] Reality Display Device Research Section, ETRI, 218 Gajeong-Ro, Yuseong-Gu, Daejeon 305-700, Republic of Korea

† Electronic supplementary information (ESI) available. See DOI: https://doi.org/10.1039/d3tc02880a

Self-aligned TFTs are considered the most suitable for high-end displays owing to their negligible parasitic capacitance. However, downsizing the oxide TFTs is critical for their application in ultra-high-resolution displays, such as VR and AR with over 3000 pixels per inch. Several strategies have been explored to reduce the footprint of TFTs.[21,22] A vertical TFT is considered as a promising candidate since it can be effectively fabricated using conventional photolithography while effectively minimizing the channel area.

A vertical TFT exhibits a bottom-contact structure, wherein the oxide semiconductor is deposited on a source/drain (S/D) electrode under an oxidizing environment.[23,24] This deposition sequence causes oxidation of the metal electrode, resulting in contact issues and degrading the output current. Particularly, the easily oxidized low-resistance Al causes a highly critical contact issue. Therefore, a capping layer of Al is necessary, and the effect of each capping layer on the contact resistance and characteristics of oxide TFTs should be investigated. The interfaces between S/D and active layers in top-contact structures have been extensively investigated.[25–28] However, the contact issues in bottom-contact structured TFTs have not been explored sufficiently.

This study analyzes the contact properties between the oxide semiconductor and metal S/D electrode in a bottom-contact structure using an Al-based metal electrode with titanium (Ti) and molybdenum (Mo) capping layers. The contact characteristics of the metal electrode are compared with those of an indium–tin oxide (ITO) non-metallic electrode, which does not exhibit contact degradation despite the oxidation of the electrode. The experiment results of the contact properties in the bottom-contact structure facilitate the realization of a vertical TFT with reasonable contact characteristics by adopting triple-layered Al-based S/D metals.

Experiments

We applied a multilayer structure to the Al-based S/D electrodes to improve their contact properties with the oxide semiconductor. The multilayered S/D electrode included Mo or Ti as capping layers. Initially, the TFTs were fabricated with a top-gate bottom-contact (TGBC) structure, as shown in Fig. 1(a), to examine the contact properties of each S/D electrode. The TGBC structure is appropriate for investigating contact properties while excluding unwanted side effects from processes, such as back-channel damage and roughness, because it has the same film stack sequences as that of a vertical TFT. The metal electrode with two types of capping layers, Mo/Al/Mo (30/100/20 nm) and Ti/Al/Ti (30/100/10 nm), served as S/D electrodes deposited via direct current (DC) sputtering on a glass substrate. The thickness of each capping layer of the bottom metal was modulated to ensure a similar sheet resistance of approximately 270 mΩ $\square^{-1}$. The high sheet resistance of the transparent oxide conductor ITO renders it unsuitable to be used as an electrode line; however, unlike metal electrodes, ITO does not exhibit any contact issue caused by oxidation. Therefore,
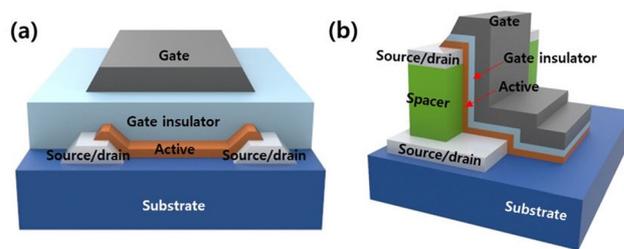
Fig. 1 Schematic of a (a) top-gate bottom-contact (TGBC) structure and (b) a vertical thin-film transistor (TFT).

the characteristics of TFTs with metal electrodes were compared with those of ITO electrodes. After the S/D patterning process, 5 nm thick InO_x active layer was deposited via plasma-enhanced atomic layer deposition (PE-ALD) at 200 °C with $Et_2InN(SiMe_3)_2$ as the precursor.[11] Subsequently, O_2 plasma treatment was performed at 7 mW mm^{-2} for 9 min to control the intrinsic carrier concentration. A 10 nm thick Al_2O_3 layer was then deposited using PE-ALD to protect the oxide semiconductor from chemical exposure.[29] A 25 nm thick Al_2O_3 layer was deposited using PE-ALD at 200 °C for the gate insulator. The influence of the external environment can be excluded without an additional passivation process owing to the outstanding barrier characteristics of the Al_2O_3 layer.[4] Finally, a 100 nm thick Mo film was deposited via DC sputtering and patterned as a gate electrode. Furthermore, the post-annealing process was performed at 200 and 250 °C for 2 h under vacuum condition. The electrical properties of each device were investigated using a semiconductor parameter analyzer (HP 4156A) in dark and 20 °C conditions to exclude the light illumination effect.[30] Based on the transfer characteristics, the contact resistance (R_{SD}) of each device was extracted using the transmission line method (TLM), and the contact properties were analyzed according to the electrode materials. We obtained the X-ray photoelectron spectroscopy (XPS) depth profiles using the K-alpha spectral line and transmission electron microscopy (TEM) images under a 200 kV electron beam energy to investigate the contact interfaces between the oxide semiconductor and S/D metals at the bottom of the device.

Finally, Al-based electrodes with capping layers were employed in vertical TFTs; the corresponding electrical performance was investigated. Fig. 1(b) shows a schematic of the fabricated vertical TFT. The Mo/Al/Mo (30/100/20 nm) or Ti/Al/Ti (30/100/10 nm) was deposited as the bottom S/D electrode on a glass substrate through DC sputtering. After patterning the bottom S/D electrode, a 500 nm-thick SiO_2 layer, which determines the channel length, was deposited through plasma-enhanced chemical vapor deposition at 300 °C. The top S/D electrode was identical to the bottom electrode. The top S/D and spacer layers were simultaneously patterned using a single photomask. The Mo/Al/Mo and Ti/Al/Ti top S/D electrodes were etched through wet- and dry-etching processes, respectively, owing to dry-etching facility issue. The active layer and gate insulator were processed similar to TGBC TFTs. The 150 nm thick Mo gate electrodes were deposited via DC sputtering and

dry-etched. The electrical characteristics of the vertical TFTs were investigated before and after thermal annealing at 200 °C.

Results and discussion

The transfer and output characteristics of the TGBC-structured oxide TFTs with different types of S/D electrodes were investigated; we evaluated the characteristics of five devices in two batches for each condition. A gate voltage (V_{gs}) ranging from −5 V to 5 V was applied at 0.1 V increments at a 0.1 V drain voltage (V_{ds}) to measure the transfer curves. Fig. 2 shows the representative transfer characteristics of the devices with widths and lengths of 20 and 10 μm, respectively, depending on the thermal annealing conditions. Fig. S1 (ESI†) shows the overlapped transfer characteristics for each sample. Table 1 summarizes the average and standard deviation values of the electrical parameters of the devices. Before thermal annealing, the device with ITO S/D electrode exhibited moderate electrical characteristics with a 27.0 cm^2 V^{-1} s^{-1} field-effect mobility (μ_{lin}). However, μ_{lin} decreased to 11.1 and 4.8 cm^2 V^{-1} s^{-1} in the devices with Mo/Al/Mo and Ti/Al/Ti metal electrodes, respectively, indicating the degradation of contact characteristics. The electrical characteristics of all TFTs improved after thermal annealing at 200 °C. The μ_{lin} in the device with Mo/Al/Mo electrode increased to 25.4 cm^2 V^{-1} s^{-1}, similar to that of the device with ITO S/D electrode at 30.5 cm^2 V^{-1} s^{-1}. Additionally, the device with the Ti/Al/Ti electrode exhibited an improved μ_{lin} of 15.4 cm^2 V^{-1} s^{-1}; however, the mobility characteristics were degraded compared with those of the device with the Mo/Al/Mo electrodes. Further annealing at a higher temperature of 250 °C caused the devices with metal S/D

electrodes to become conductive or exhibit negatively shifted behavior. By contrast, the device with the ITO S/D electrode maintained its on/off characteristics.

The output curves of each device were measured and investigated in the low-V_{ds} region to compare the contact properties based on the S/D electrode materials. The output characteristics were measured by applying V_{ds}, ranging from −1 V to 10 V, with various values of V_{gs} (0, 1, 3 and 5 V). Fig. 3(a)–(c) show the output curves of the TGBC TFTs with Mo/Al/Mo, Ti/Al/Ti, and ITO S/D electrodes, respectively, before thermal annealing. As indicated in the previously obtained transfer characteristics, the devices with Mo/Al/Mo and Ti/Al/Ti electrodes exhibited a low output current. Particularly, a nonlinear relationship was observed between the drain current and drain voltage when V_{ds} was approximately 0 V (insets of output curves). The TFT with the Ti/Al/Ti S/D electrode exhibited the lowest current, with the slope indicating a sagged shape; this indicates the presence of contact issues and Schottky barrier tunneling between the active layer and S/D electrode.[25] After thermal annealing at 200 °C, the output characteristics of the devices with metal electrodes remarkably improved and were similar to those of the devices with ITO S/D electrodes (Fig. 3(d)–(f)).

The R_{SD} values of the devices were calculated using TLM[31] based on their electrical characteristics, as follows:

$$R_{tot} = \frac{V_{ds}}{I_{ds}}, \tag{1}$$

$$R_{tot}W = R_S L + R_{SD}W = \frac{L}{\mu C_i(V_{gs} - V_{on})} + R_{SD}W, \tag{2}$$

where R_{tot}, R_S, V_{on}, L, and W indicate the total resistance, sheet resistance, turn-on voltage, channel length, and width, respectively. The R_{tot} can be derived using Ohm's law and can be calculated with the drain current (I_{ds}) at specific V_{gs} and V_{ds} (0.1 V) from the transfer curves in the linear region. The channel width was maintained constant at 20 μm, whereas the channel length was varied at 5, 10, 15, 20, 25, and 30 μm. The $R_{tot}W$ exhibited a linear relationship with the channel length for a constant value of V_{gs} (Fig. S1, ESI†). Based on the $R_{tot}W$ versus L curves, the R_{SD} of each device was extracted using $V_{gs} - V_{on}$, as shown in Fig. 4. The TFTs exhibited lower contact resistances because the applied V_{gs} was high owing to the increased carrier density. Before annealing, the R_{SD} values of the TFTs with Mo/Al/Mo, Ti/Al/Ti, and ITO S/D electrodes were 59, 243, and 2.4 kΩ, respectively, at $V_{gs} - V_{on} = 4$ V. After thermal annealing at 200 °C, the R_{SD} values of the Mo/Al/Mo, Ti/Al/Ti, and ITO S/D
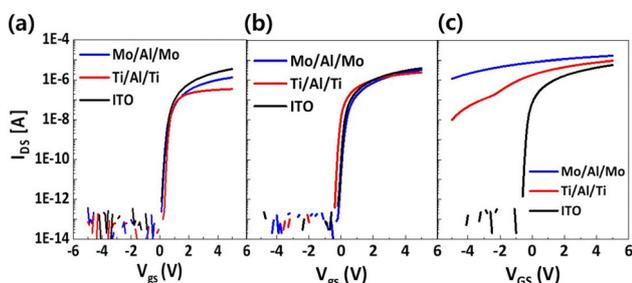
Fig. 2 Transfer characteristics of the top-gate bottom-contact (TGBC) thin-film transistors (TFTs) with different types of source/drain (S/D) electrodes. (a) Before annealing and after vacuum annealing at (b) 200 °C and (c) 250 °C.

Table 1 Average and standard deviation values of the electrical parameters of five TGBC TFTs with different types of S/D electrodes before and after thermal annealing

S/D electrode materials		S.S [V dec^{-1}]	V_{on} [V]	Hys. [V]	μ_{lin} [cm^2 V^{-1} s^{-1}]	ON/OFF ($\times 10^7$)
Mo/Al/Mo	Before annealing	0.09 ± 0.00	0.28 ± 0.03	0.62 ± 0.08	0.62 ± 0.08	2.09 ± 1.04
	Annealed at 200 °C	0.08 ± 0.01	0.02 ± 0.04	0.24 ± 0.09	0.24 ± 0.09	3.46 ± 1.66
Ti/Al/Ti	Before annealing	0.07 ± 0.01	0.21 ± 0.16	0.76 ± 0.05	0.76 ± 0.05	0.45 ± 0.03
	Annealed at 200 °C	0.07 ± 0.01	−0.30 ± 0.05	0.30 ± 0.07	0.30 ± 0.07	0.79 ± 1.11
ITO	Before annealing	0.10 ± 0.01	0.20 ± 0.03	0.56 ± 0.18	0.56 ± 0.18	2.55 ± 1.80
	Annealed at 200 °C	0.07 ± 0.01	−0.14 ± 0.14	0.48 ± 0.19	0.48 ± 0.19	4.68 ± 2.08
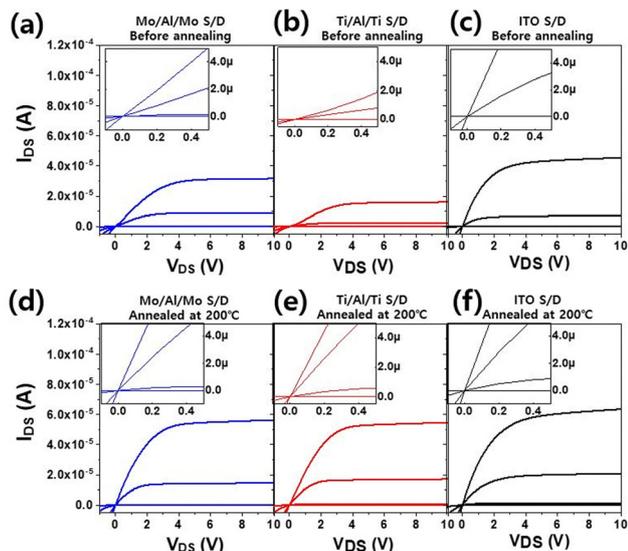
Fig. 3 Output curves of the top-gate bottom-contact (TGBC) thin-film transistors (TFTs) with (a) Mo/Al/Mo, (b) Ti/Al/Ti, and (c) indium–tin oxide (ITO) electrodes before annealing. Output curves of the devices with (d) Mo/Al/Mo, (e) Ti/Al/Ti, and (f) ITO electrodes after annealing at 200 °C.
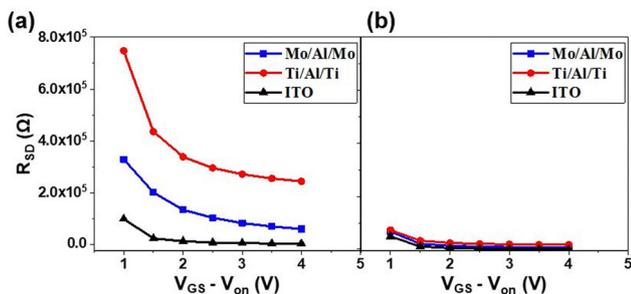
Fig. 4 Extracted contact resistance (R_{SD}) calculated as the difference between the gate voltage and turn-on voltage ($V_{gs} - V_{on}$) using the transmission line method (TLM) in the top-gate bottom-contact (TGBC) thin-film transistors (TFTs) with Mo/Al/Mo, Ti/Al/Ti, and indium–tin oxide (ITO) electrodes (a) before and (b) after annealing at 200 °C.

TFTs significantly reduced to 5.7, 17, and 0.2 kΩ, respectively. The additional carriers generated in the oxide semiconductor after thermal annealing improved the contact properties. Furthermore, indium-rich regions were formed at the interface between the metal and InO$_x$. The bond between indium and oxygen in the contact region was broken, and the oxygen atoms within the semiconductor of InO$_x$ bonded with the S/D metals to form metal oxides. Consequently, many oxygen vacancies were generated within the InO$_x$. Typically, the oxygen vacancies in the oxide semiconductor serve as shallow donors to generate electrons, increasing the carrier density.[32] Therefore, the contact resistances decrease after thermal annealing; further annealing at higher temperatures causes substantial carrier generation, inducing a negative shift in V_{on}.

We analyzed the band alignments of the contact structures to investigate the contact properties between the InO$_x$ active layer and each S/D electrode. The work function and valence
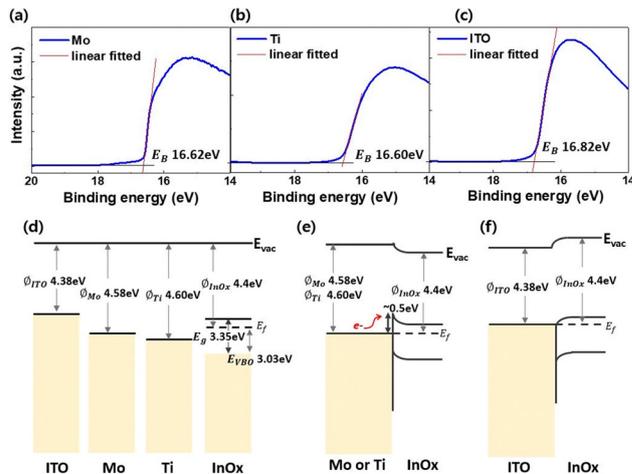
Fig. 5 Ultraviolet photoelectron spectroscopy (UPS) spectra of (a) Mo, (b) Ti, and (c) indium–tin oxide (ITO) to determine the work function. (d) Schematic of the band position of electrode materials and InO$_x$. Band alignment in the contact between (e) Mo/InO$_x$ or Ti/InO$_x$ and (f) ITO/InO$_x$.

band offset (VBO) of each material were measured through ultraviolet photoelectron spectroscopy (UPS). Fig. 5(a)–(c) show the UPS-measured data of Mo, Ti, and ITO electrodes, respectively, at a high binding energy. The work function can be calculated as[33]

$$\varnothing = h\nu - E_B \text{ (secondary cut-off)}, \qquad (3)$$

where Φ, $h\nu$, and E_B represent the work function, incident photon energy, and binding energy, respectively. We considered He-I UPS with a 21.2 eV energy in our analysis. Fig. 5(d) shows a schematic of the band position of electrode materials and InO$_x$, including work function, band-gap energy (E_g), and VBO. We determined the values of E_B and VBO of InO$_x$ using UPS and the E_g extracted from the transmission spectra measured *via* ultraviolet-visible measurement (Fig. S2, ESI†).[34–36] Mo and Ti exhibited larger work functions than InO$_x$; therefore, the Schottky barrier was generated when they were in contact (Fig. 5(e)). Based on the extracted E_g, VBO, and work function values, the estimated height of the Schottky barrier was approximately 0.5 eV.[37] Therefore, the devices with Mo/Al/Mo and Ti/Al/Ti S/D electrodes exhibited degraded transfer and output characteristics before thermal annealing. Conversely, the ITO S/D electrodes formed an ohmic contact with InO$_x$ (Fig. 5(f)), resulting in an oxide TFT with reasonable electrical properties without contact issues. Although the Schottky junction is formed in the Mo or Ti metal and InO$_x$ interfaces, oxide TFTs with high carrier concentration exhibit adequate electrical characteristics when appropriate forward V_{gs} and V_{ds} are applied, and the barrier height can be surpassed.[38,39]

The bonding states at the interfaces between the metal and oxide semiconductors were investigated through XPS by analyzing the metal peaks. Fig. 6(a) and (b) show the Mo 3d and Ti 2p metal peaks, respectively, in the bulk metal region (black line) and contact region (blue line). The approximate contact regions were determined through XPS depth profiles by observing a

decrease in the atomic ratio of indium and an increase in the metal content (Mo or Ti) up to a certain extent.[40] Additionally, because the oxygen stoichiometry in MoO_2 or TiO_2 was larger than in In_2O_3, we considered the regions where the oxygen depth profile increased and saturated as the contact region (Fig. S4, ESI†). A few shoulder peaks were generated in the contact region of the Mo/Al/Mo and Ti/Al/Ti electrodes, unlike in the bulk metal region. This implies that Mo and Ti at the contact interface have various oxidation states, indicating the possible oxidation of certain metals in the contact region. An additional Ti_2O_3 peak was observed with significant broadening in the Ti/Al/Ti electrode, implying the formation of TiO_x at the contact interface.[41] Furthermore, no significant variation in the Ti sub-peaks was observed within the proximity of the contact regions, regardless of the depth sputtering time, as shown in Fig. S4 (ESI†). However, the data of XPS peaks included bonding state information up to the depth of several tens of micrometers, limiting the use of XPS for comparing the degree of oxidation.

Fig. 6(c) and (d) show the cross-sections of each sample analyzed using TEM to compare the degree of oxidation at the contact interfaces *via* structural analysis. No metal oxides were formed in the the Mo/InO_x interface. However, an additional layer was observed between the Ti and InO_x layers. Based on the energy dispersive spectroscopy (EDS) analysis, the Ti elements were detected in these interlayer regions (Fig. S3, ESI†); the TiO_x layer formed at the interface between Ti and InO_x degraded the contact properties.

The difference in the degree of oxidation under the same conditions between Mo and Ti metals can be attributed to thermodynamic reasons. The thermodynamic stability of a metal–oxide interface can be calculated using tabulated standard free energy of formation data. The Gibbs free energy (ΔG^0_{rxn}) of the reactions of Mo, Ti, and Al with In_2O_3 at 200 °C are expressed as[42,43]

$$3Mo_{(s)} + 2In_2O_{3(s)} = 4In_{(l)} + 3MoO_{2(s)} \quad \Delta G^0_{rxn} = 24.6 \text{ kJ mol}^{-1}, \tag{4}$$

$$3Ti_{(s)} + 2In_2O_{3(s)} = 4In_{(l)} + 3TiO_{2(s)} \quad \Delta G^0_{rxn} = -509.7 \text{ kJ mol}^{-1}, \tag{5}$$

$$3Al_{(s)} + In_2O_{3(s)} = 2In_{(l)} + Al_2O_{3(s)} \quad \Delta G^0_{rxn} = -752.6 \text{ kJ mol}^{-1}. \tag{6}$$
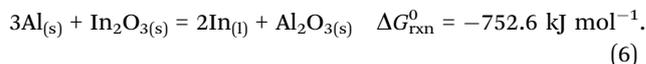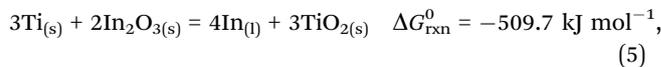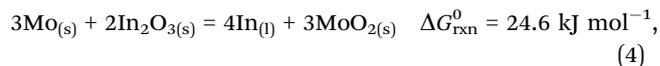
The ΔG^0_{rxn} of each reaction was compared at 200 °C, which denotes the deposition temperature of InO_x at which the metal–oxide semiconductor interface is formed. The reaction between Mo and In_2O_3 to form MoO_2 exhibits a positive ΔG^0_{rxn} value of 24.6 kJ mol^{-1},[42] indicating that additional energy is required. By contrast, the reaction between Ti and In_2O_3 to form TiO_2 exhibits a large negative ΔG^0_{rxn} value of −509.7 kJ mol^{-1},[42,43] indicating that TiO_2 formation is more thermodynamically stable than the existing Ti metal in the contact region at 200 °C.[43] Therefore, the formation of TiO_2 was more thermodynamically stable than that of MoO_2 in the deposition environment of InO_x. Consequently, the metal–oxide layer was more apparent in the cross-sectional TEM images. This indicates that electrical devices suffer from contact issues when TFTs are used with Ti/Al/Ti electrodes. The Al oxidation at the contact interface with In_2O_3 was a thermodynamically stable reaction with a larger negative value (−752.6 kJ mol^{-1}) than that of the Ti oxidation reaction. Furthermore, Al oxidation was apparent at the interface between InO_x and Al metal when the InO_x was directly deposited on the Al metal surface (Fig. S4, ESI†). Therefore, oxide TFTs with Al electrodes require additional capping layers to exhibit a normal electrical performance.[44]

We fabricated and investigated the performance of vertical TFTs with Al-based metal electrodes according to the results of the TGBC TFTs. Fig. 7(a) and (b) compare the transfer characteristics of vertical TFTs with Mo/Al/Mo and Ti/Al/Ti electrodes before and after thermal annealing, respectively. The width and length of the vertical TFTs were 8 and 0.5 μm, respectively. The vertical TFTs demonstrated an improvement in the OFF-current after thermal annealing. In vertical TFTs, the electrical characteristics are closely related to the back-channel properties. In particular, the processes involved in the dry etching of spacers and the ashing process for photoresist (PR) removal can generate defects within the back-channel. These defects increase the intrinsic carrier concentration within the adjacent active layers, elevating the OFF-current, as documented in prior studies.[23] Subsequent thermal annealing rectify these defects, enhancing the OFF-current performance.

The vertical TFTs exhibited severe contact issues before thermal annealing, similar to that observed in the TGBC TFTs. After thermal annealing at 200 °C, the electrical performances of the vertical TFTs significantly improved. However, the vertical TFT with Mo/Al/Mo electrodes exhibited substantially better electrical characteristics than that with Ti/Al/Ti electrodes, wherein the current flow was degraded, and a negative
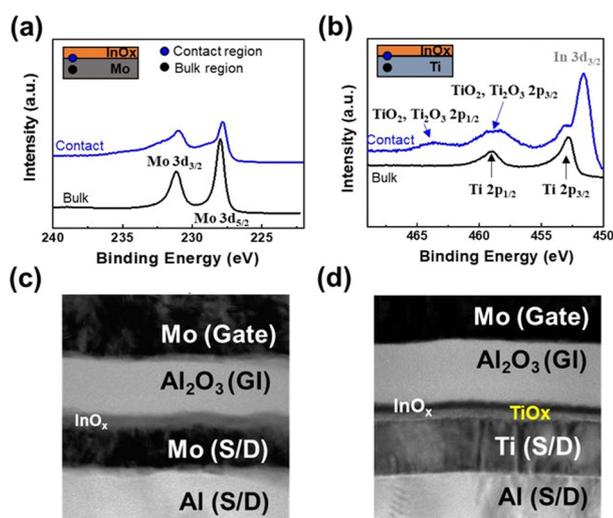
Fig. 6 X-ray photoelectron spectroscopy (XPS) spectra of metal peaks (a) Mo 3d and (b) Ti 2p in the bulk metal region (black line) and contact region (blue line). Cross-sectional high-resolution transmission electron microscopy (TEM) images of the contact region of the top-gate bottom-contact (TGBC) thin-film transistors (TFTs) with (c) Mo/Al/Mo and (d) Ti/Al/Ti source/drain (S/D) electrodes.
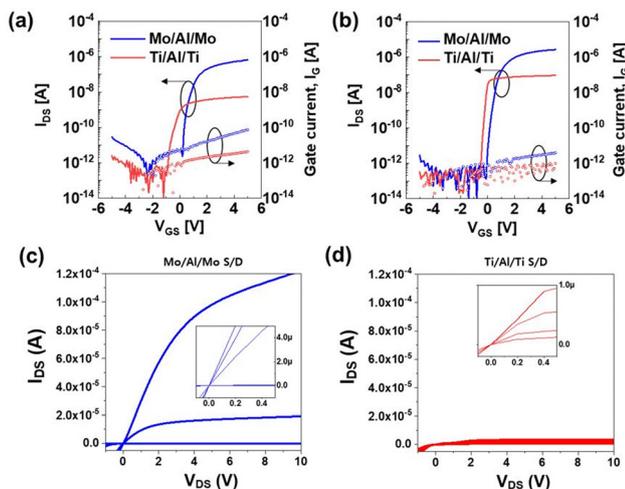
Fig. 7 Transfer characteristics of vertical thin-film transistors (TFT) with Mo/Al/Mo and Ti/Al/Ti source/drain (S/D) electrodes (a) before and (b) after thermal annealing at 200 °C. Output curves of the vertical TFTs with (c) Mo/Al/Mo and (d) Ti/Al/Ti S/D after thermal annealing at 200 °C.

Fig. 8 Cross-sectional transmission electron microscopy (TEM) images of the fabricated vertical TFTs with (a) Mo/Al/Mo and (b) Ti/Al/Ti S/D electrodes.

shift was observed at V_{on}. As discussed earlier, the contact between Ti and InO_x exhibited less favorable characteristics in terms of electrode oxidation compared with that between Mo and InO_x. Therefore, the vertical TFT with Ti/Al/Ti electrodes presented severe contact issues and a negative V_{on} shift, originating from the generation of oxygen vacancies in InO_x during the formation of TiO_x. The vertical TFTs exhibited a relatively high gate leakage current before thermal annealing but decreased to below 10 pA after thermal annealing. However, it remained slightly higher than that of the TGBC TFTs, with approximately 1 pA of leakage current (Fig. 2). This difference may be attributed to the roughness degradation of the back channel in the vertical TFTs caused by the dry etching of spacers. This degradation could introduce leakage paths for tunneling current, particularly when using a thin gate insulator.[23] Further improvements can be achieved by optimizing the etching process of the spacers or applying additional treatments, such as oxygen plasma treatment.

The output curves of each vertical TFTs were measured under the same condition as that for TGBC TFTs. Fig. 7(c) and (d) show the output curves after thermal annealing at 200 °C of the vertical TFTs with Mo/Al/Mo and Ti/Al/Ti S/D electrodes, respectively. As previously observed in the transfer curves, the devices with Ti/Al/Ti electrodes exhibited extremely low output current owing to the oxidation of Ti. By contrast, the vertical TFT with Mo/Al/Mo electrodes exhibited reasonable output characteristics. Notably, the vertical TFT with Mo/Al/Mo electrodes demonstrated a larger output current than the TGBC TFTs, despite the degraded electrical parameters. This is attributed to the extremely short channel length of the vertical TFTs, which operates on a nanometer scale. Furthermore, this extremely short channel length made it difficult for the output current to saturate with an increased V_{ds} owing to the drain-induced barrier lowering effect.[45]

Structural analysis was performed based on the TEM images of the cross-sectional structure of each vertical TFT (Fig. 8(a)
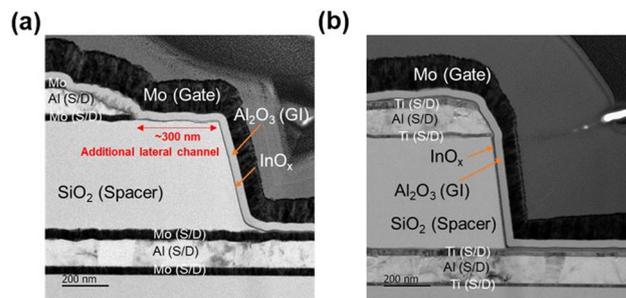
and (b)). This study used ALD for the deposition of the InO_x active layer, resulting in excellent step coverage throughout the three-dimensional structure. Consequently, any concerns related to asymmetric thickness distribution of the active layer, which can be an issue with sputtering methods, can be confidently excluded.[46] The isotropic Mo/Al/Mo wet-etching process caused undercutting, resulting in the lateral etching of the top Mo/Al/Mo S/D electrode above the spacer by approximately 300 nm; an additional channel length was also formed (Fig. 7(c)). By contrast, because the top Ti/Al/Ti S/D electrode was dry-etched using a Cl-based etching gas,[47] the channel layer was formed vertically along the spacer. The vertical TFTs exhibited slightly degraded electrical properties compared with those of the previously investigated TGBC TFTs. The back channel of the vertical oxide TFT was exposed through the dry-etching process during the spacer formation. Consequently, the roughness of the spacer degraded the electrical properties of the vertical TFT with a thin active layer of InO_x.[48] Furthermore, unwanted byproducts were introduced into the back channel during the dry-etching of the spacer, affecting the oxide semiconductors.

Table 2 summarizes the electrical parameters of the vertical TFTs extracted considering the actual channel dimensions. Before thermal annealing, the field-effect mobilities of vertical TFTs with Mo/Al/Mo and Ti/Al/Ti S/D electrodes were 0.77 and 0.002 cm^2 V^{-1} s^{-1}, respectively. After annealing at 200 °C, the Mo/Al/Mo vertical TFT exhibited significant improvement in ON-current, hysteresis, and μ_{lin}, whereas the Ti/Al/Ti vertical TFT exhibited only a slight improvement. As the channel length of a vertical TFT is determined using the thickness of the spacer, investigating the electrical characteristics becomes difficult with varying channel lengths. Therefore, the contact resistance must be extracted using TLM and other novel methods. In this study, R_{SD} was extracted according to the schematic shown in the inset in Fig. 9 and using the following equations:

$$V_{GS} = V_{gs} - I_{ds}R_{S}, \quad (7)$$

$$V_{DS} = V_{ds} - I_{ds}R_{S} - I_{ds}R_{D} = V_{ds} - I_{ds}R_{SD}, \quad (8)$$

where V_{GS} and V_{DS} indicate the applied gate and drain voltages to the channel, respectively, considering the effect of series

Table 2 Average and standard deviation values of the electrical parameters of five vertical TFTs with Mo/Al/Mo and Ti/Al/Ti S/D electrodes, including S.S, V_{on}, hysteresis, and field-effect mobility

S/D electrode materials		S.S [V dec^{-1}]	V_{on} [V]	Hys. [V]	μ_{lin} [cm^2 V^{-1} s^{-1}]
Mo/Al/Mo	Before annealing	0.13 ± 0.01	0.45 ± 0.09	0.80 ± 0.11	0.77 ± 0.06
	Annealed at 200 °C	0.13 ± 0.01	0.14 ± 0.05	0.26 ± 0.05	3.26 ± 0.45
Ti/Al/Ti	Before annealing	0.39 ± 0.07	−0.43 ± 0.11	0.23 ± 0.11	0.002 ± 0.001
	Annealed at 200 °C	0.10 ± 0.02	−0.29 ± 0.18	0.22 ± 0.05	0.05 ± 0.06

resistance and parasitic capacitance on the applied bias to the gate (V_{gs}) and drain (V_{ds}) electrodes. In the case of large V_{GS} and extremely small V_{DS}, the V_{gs} and V_{ds} can be expressed as

$$V_{GS} \cong V_{gs}, \tag{9}$$

$$V_{GS} - V_{th} - \frac{1}{2}V_{DS} \cong V_{GS} - V_{th}. \tag{10}$$

As V_{GS} was assumed to be large, and V_{DS} was sufficiently small, the above equation can be applied to the relationship equation between the drain current (I_{ds}) and V_{GS} in the linear region, as follows:[49,50]

$$I_{ds} = \frac{W \cdot C_{ox}}{L} \cdot \mu \cdot \left(V_{gs} - V_{th}\right) \cdot \left(V_{DS}\right), \tag{11}$$

$$I_{ds} = \frac{W \cdot C_{ox}}{L} \cdot \mu \cdot \left(V_{gs} - V_{th}\right) \cdot \left(V_{ds} - I_{ds}R_{SD}\right), \tag{12}$$

$$I_{ds} = m \cdot (V_{gs} - V_{th}) \cdot (V_{ds} - I_{ds}R_{SD}), \tag{13}$$

$$\frac{V_{ds}}{I_{ds}} = \frac{1}{m(V_{GS} - V_{th})} + R_{SD}, \tag{14}$$

where C_{ox}, μ, and V_{th} indicate the gate dielectric capacitance, charge carrier mobility, and threshold voltage, respectively. As the V_{ds}/I_{ds} has a linear relationship with $1/(V_{GS} - V_{th})$, we can obtain the R_{SD} from the y-intercept of the linear graph of V_{ds}/I_{ds} *versus* $1/(V_{GS} - V_{th})$. Fig. 9 shows the linear graphs of the Mo/Al/Mo and Ti/Al/Ti vertical TFTs. The extracted R_{SD} values from the vertical TFT with Mo/Al/Mo and Ti/Al/Ti electrodes were 15 and 984 kΩ, respectively, higher than those obtained from the TGBC TFTs. The exposure of the top surface and side

Fig. 9 Linear relationship between V_{ds}/I_{ds} and $1/(V_{GS} - V_{th})$ of the vertical thin-film transistor (TFT) with Mo/Al/Mo and Ti/Al/Ti source/drain (S/D) electrodes.

plane of electrodes to the dry-etching process of the spacer can degrade the morphology and resistive characteristics of the metal electrode. Therefore, we inferred that the contact properties of Mo/Al/Mo and Ti/Al/Ti in vertical TFTs were degraded compared with those of the TGBC TFTs.

The electrical properties of the vertical TFT strongly rely on the electrode materials. This emphasizes the importance of carefully considering electrode materials and their structure for realizing high-end vertical TFTs. Further research is necessary to develop metal-based materials with low resistance and adequate contact properties based on oxide semiconductors in bottom-contact structures to improve the electrical properties of vertical TFTs.

Conclusions

This study investigated the bottom-contact properties of Al-based electrodes with Mo and Ti capping layers to achieve reasonable performances of vertical TFTs. We analyzed the contact properties of Mo/Al/Mo and Ti/Al/Ti electrodes with InO$_x$ by fabricating TGBC-structured TFTs. Before thermal annealing, the TGBC TFT with metal electrodes exhibited contact issues, whereas the device with ITO electrodes exhibited normal electrical characteristics. After thermal annealing at 200 °C, the electrical characteristics of the devices with Mo/Al/Mo and Ti/Al/Ti electrodes were improved. The R_{SD} values of each device were extracted and compared using TLM. The results indicated that the contact resistance of the Ti/Al/Ti electrodes was high before thermal annealing. The band alignment between each capping metal and InO$_x$ was investigated based on the UPS measurements. The results indicated that the Mo and Ti metals formed a Schottky contact with InO$_x$, whereas the ITO formed an ohmic contact. Additionally, the results of the XPS depth profile and TEM analysis confirmed the formation of TiO$_x$ at the contact interface. Finally, based on the analysis of the TGBC TFTs, the Al-based electrodes were adopted in the vertical TFTs. The vertical TFT with Mo/Al/Mo S/D electrodes exhibited electrical performance with a field-effect mobility of 3.3 cm^2 V^{-1} s^{-1} at a turn-on voltage of 0.14 V. The vertical TFTs exhibited degraded electrical characteristics compared with those of the TGBC TFTs owing to process side effects, including the degradation caused by the rough morphology resulting from the dry-etching process in the back channel and the outgassing from the spacer. Our analysis revealed that electrode materials significantly influence the performance of vertical TFTs. Therefore, carefully considering electrode materials and their structure is crucial for designing
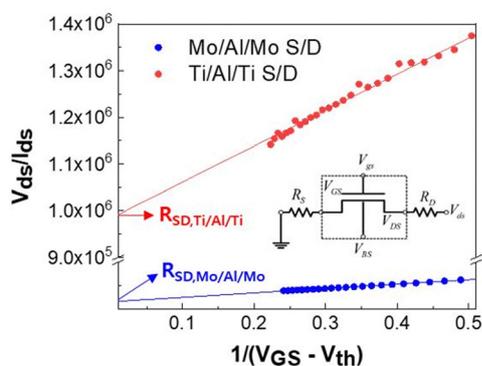
high-end vertical TFTs. These study findings can facilitate the development of vertical TFTs with reduced RC delays for ultra-high-resolution display applications.

Author contributions

Sori Jeon: conceptualization, methodology, investigation, writing – original draft; Kwang-Heum Lee: formal analysis, investigation; Seung-Hee Lee: formal analysis, investigation; Seong-In Cho: investigation, writing – review & editing; Chi-Sun Hwang: methodology, investigation; Jong Beom Ko: conceptualization, investigation, writing – review & editing; Sang-Hee Ko Park: supervision, funding acquisition, writing – review & editing.

Conflicts of interest

There are no conflicts to declare.

Acknowledgements

References

1 L. D. Xu, W. He and S. C. Li, Internet of Things in Industries: A Survey, *IEEE Trans. Ind. Inform.*, 2014, **10**(4), 2233–2243, DOI: **10.1109/Tii.2014.2300753**.

2 D. Prattichizzo, F. Chinello, C. Pacchierotti and M. Malvezzi, Towards Wearability in Fingertip Haptics: A 3-DoF Wearable Device for Cutaneous Force Feedback, *IEEE Trans. Haptics*, 2013, **6**(4), 506–516, DOI: **10.1109/ToH.2013.53**.

3 J. B. Ko, S. H. Lee, T. I. Lee, S. Lee, J. Kim, H. Kim, T. S. Kim and S. H. K. Park, Ultrathin, Flexible, and Transparent Oxide Thin-Film Transistors by Delamination and Transfer Methods for Deformable Displays, *Adv. Mater. Technol.*, 2021, **6**(11), 2100431, DOI: **10.1002/admt.202100431**.

4 J. B. Ko, S. H. Lee, K. W. Park and S. H. K. Park, Interface tailoring through the supply of optimized oxygen and hydrogen to semiconductors for highly stable top-gate-structured high-mobility oxide thin-film transistors, *RSC Adv.*, 2019, **9**(62), 36293–36300, DOI: **10.1039/c9ra06960g**.

5 J. Y. Kwon, K. S. Son, J. S. Jung, T. S. Kim, M. K. Ryu, K. B. Park, B. W. Yoo, J. W. Kim, Y. G. Lee, K. C. Park, S. Y. Lee and J. M. Kim, Bottom-Gate Gallium Indium Zinc Oxide Thin-Film Transistor Array for High-Resolution AMOLED Display, *IEEE Electron Device Lett.*, 2008, **29**(12), 1309–1311, DOI: **10.1109/Led.2008.2006637**.

6 J. S. Park, W. J. Maeng, H. S. Kim and J. S. Park, Review of recent developments in amorphous oxide semiconductor thin-film transistor devices, *Thin Solid Films*, 2012, **520**(6), 1679–1693, DOI: **10.1016/j.tsf.2011.07.018**.

7 M. Nakata, C. M. Zhao and J. Kanicki, DC sputtered amorphous In-Sn-Zn-O thin-film transistors: Electrical properties and stability, *Solid State Electron.*, 2016, **116**, 22–29, DOI: **10.1016/j.sse.2015.11.025**.

8 Z. T. Ao, F. Shan, H. B. Guo, H. S. Kim, J. Y. Lee and S. J. Kim, Indium Zinc Oxide Thin-Film Transistors with Ultraviolet Post-Annealing Treatment, *J. Nanosci. Nanotechnol.*, 2019, **19**(10), 6170–6173, DOI: **10.1166/jnn.2019.16996**.

9 E. Fortunato, P. Barquinha, G. Goncalves, L. Pereira and R. Martins, High mobility and low threshold voltage transparent thin film transistors based on amorphous indium zinc oxide semiconductors, *Solid State Electron.*, 2008, **52**(3), 443–448, DOI: **10.1016/j.sse.2007.10.032**.

10 B. K. Kim, N. On, C. H. Choi, M. J. Kim, S. Kang, J. H. Lim and J. K. Jeong, Polycrystalline Indium Gallium Tin Oxide Thin-Film Transistors With High Mobility Exceeding 100 cm(2)/Vs, *IEEE Electron Device Lett.*, 2021, **42**(3), 347–350, DOI: **10.1109/Led.2021.3055940**.

11 H. I. Yeom, J. B. Ko, G. Mun and S. H. K. Park, High mobility polycrystalline indium oxide thin-film transistors by means of plasma-enhanced atomic layer deposition, *J. Mater. Chem. C*, 2016, **4**(28), 6873–6880, DOI: **10.1039/c6tc00580b**.

12 C. L. Fan, F. P. Tseng and C. Y. Tseng, Electrical Performance and Reliability Improvement of Amorphous-Indium-Gallium-Zinc-Oxide Thin-Film Transistors with HfO2 Gate Dielectrics by CF4 Plasma Treatment, *Materials*, 2018, **11**(5), 824, DOI: **10.3390/ma11050824**.

13 S. J. Park and T. J. Ha, Improved electric contact of recessed source and drain electrodes for sol-gel-based thin-film transistors consisting of amorphous ZrO2 and IGZO fabricated by microwave-annealing, *Appl. Phys. Lett.*, 2022, **120**(15), 153301, DOI: **10.1063/5.0086833**.

14 Y. Nam, H. O. Kim, S. H. Cho and S. H. K. Park, Effect of hydrogen diffusion in an In-Ga-Zn-O thin film transistor with an aluminum oxide gate insulator on its electrical properties, *RSC Adv.*, 2018, **8**(10), 5622–5628, DOI: **10.1039/c7ra12841j**.

15 Y. M. Kim and G. W. Lee, Effects of Al₂O₃ gate insulator on the instability of amorphous indium-gallium zinc oxide thin film transistors, *AIP Adv.*, 2018, **8**(8), 085112, DOI: **10.1063/1.5043340**.

16 M. J. Zhao, M. Xu, H. L. Ning, R. X. Xu, J. H. Zou, H. Tao, L. Wang and J. B. Peng, Method for Fabricating Amorphous Indium-Zinc-Oxide Thin-Film Transistors With Copper Source and Drain Electrodes, *IEEE Electron Device Lett.*, 2015, **36**(4), 342–344, DOI: **10.1109/Led.2015.2400632**.

17 G. Koren, F. Ho and J. J. Ritsko, Excimer Laser Etching of Al Metal-Films in Chlorine Environments, *Appl. Phys. Lett.*, 1985, **46**(10), 1006–1008, DOI: **10.1063/1.95815**.

18 J. I. Park, Y. Lim, M. Jang, S. I. Choi, N. Hwang and M. Yi, Improved stability of aluminum co-sputtered indium zinc oxide thin-film transistor, *Mater. Res. Bull.*, 2017, **96**, 155–159, DOI: **10.1016/j.materresbull.2017.05.001**.

19 W. Jeong, J. Winkler, H. Schmidt, K. H. Lee and S. H. K. Park, Suppressing channel-shortening effect of self-aligned coplanar Al-doped In-Sn-Zn-O TFTs using Mo-Al alloy

source/drain electrode as Cu diffusion barrier, *J. Alloys Compd.*, 2021, **859**, 158227, DOI: **10.1016/j.jallcom.2020.158227**.

20 P. Barquinha, A. M. Vila, G. Goncalves, R. Martins, J. R. Morante, E. Fortunato and L. Pereira, Gallium-indium-zinc-oxide-based thin-film transistors: Influence of the source/drain material, *IEEE Trans. Electron Devices*, 2008, **55**(4), 954–960, DOI: **10.1109/Ted.2008.916717**.

21 J. H. Choi, J. H. Yang, J. E. Pi, C. Y. Hwang, Y. H. Kim, G. H. Kim, H. O. Kim and C. S. Hwang, The new route for realization of 1-mu m-pixel-pitch high-resolution displays, *J. Soc. Inf. Disp.*, 2019, **27**(8), 487–496, DOI: **10.1002/jsid.821**.

22 S. Katsui, H. Kobayashi, T. Nakagawa, Y. Tamatsukuri, H. Shishido, S. Uesaka, R. Yamaoka, T. Nagata, T. Aoyama, K. Nei, Y. Okazaki, T. Ikeda and S. Yamazaki, A 5291-ppi organic light-emitting diode display using field-effect transistors including a c-axis aligned crystalline oxide semiconductor, *J. Soc. Inf. Disp.*, 2019, **27**(8), 497–506, DOI: **10.1002/jsid.822**.

23 C. S. Hwang, S. H. K. Park, H. Oh, M. K. Ryu, K. I. Cho and S. M. Yoon, Vertical Channel ZnO Thin-Film Transistors Using an Atomic Layer Deposition Method, *IEEE Electron Device Lett.*, 2014, **35**(3), 360–362, DOI: **10.1109/Led.2013.2296604**.

24 K. G. Sun, S. F. Nelson and T. N. Jackson, Modeling of Self-Aligned Vertical ZnO Thin-Film Transistors, *IEEE Trans. Electron Devices*, 2015, **62**(6), 1912–1917, DOI: **10.1109/Ted.2015.2418174**.

25 Y. Shimura, K. Nomura, H. Yanagi, T. Kamiya, M. Hirano and H. Hosono, Specific contact resistances between amorphous oxide semiconductor In-Ga-Zn-O and metallic electrodes, *Thin Solid Films*, 2008, **516**(17), 5899–5902, DOI: **10.1016/j.tsf.2007.10.051**.

26 Y. Ueoka, Y. Ishikawa, J. P. Bermundo, H. Yamazaki, S. Urakawa, Y. Osada, M. Horita and Y. Uraoka, Effect of contact material on amorphous InGaZnO thin-film transistor characteristics, *Jpn. J. Appl. Phys.*, 2014, **53**(3), 03cc04, DOI: **10.7567/Jjap.53.03cc04**.

27 H. Park, J. Yun, S. Park, I. S. Ahn, G. Shin, S. Seong, H. J. Song and Y. Chung, Enhancing the Contact between a-IGZO and Metal by Hydrogen Plasma Treatment for a High-Speed Varactor (>30 GHz), *ACS Appl. Electron. Mater.*, 2022, **4**(4), 1769–1775, DOI: **10.1021/acsaelm.2c00028**.

28 M. Nag, A. Bhoolokam, S. Steudel, A. Chasin, K. Myny, J. Maas, G. Groeseneken and P. Heremans, Back-channel-etch amorphous indium-gallium-zinc oxide thin-film transistors: The impact of source/drain metal etch and final passivation, *Jpn. J. Appl. Phys.*, 2014, **53**(11), 111401, DOI: **10.7567/Jjap.53.111401**.

29 J. B. Ko, H. I. Yeom and S. H. K. Park, Plasma-Enhanced Atomic Layer Deposition Processed SiO2 Gate Insulating Layer for High Mobility Top-Gate Structured Oxide Thin-Film Transistors, *IEEE Electron Device Lett.*, 2016, **37**(1), 39–42, DOI: **10.1109/Led.2015.2504931**.

30 P. Barquinha, A. Pimentel, A. Marques, L. Pereira, R. Martins and E. Fortunato, Effect of UV and visible light radiation on the electrical performances of transparent TFTs based on amorphous indium zinc oxide, *J. Non-Cryst. Solids*, 2006, **352**(9–20), 1756–1760, DOI: **10.1016/j.jnoncrysol.2006.01.068**.

31 W. Wang, L. Li, C. Y. Lu, Y. Liu, H. B. Lv, G. W. Xu, Z. Y. Ji and M. Liu, Analysis of the contact resistance in amorphous InGaZnO thin film transistors, *Appl. Phys. Lett.*, 2015, **107**(6), 063504, DOI: **10.1063/1.4928626**.

32 J. Jang, Y. Kang, D. Cha, J. Bae and S. Lee, Thin-Film Optical Devices Based on Transparent Conducting Oxides: Physical Mechanisms and Applications, *Crystals*, 2019, **9**(4), 192, DOI: **10.3390/cryst9040192**.

33 Y. H. Joo, J. H. Wi, W. J. Lee, Y. D. Chung, D. H. Cho, S. Kang, D. S. Um and C. I. Kim, Work Function Tuning of Zinc-Tin Oxide Thin Films Using High-Density O-2 Plasma Treatment, *Coatings*, 2020, **10**(11), 1026, DOI: **10.3390/coatings10111026**.

34 A. Klein, C. Korber, A. Wachau, F. Sauberlich, Y. Gassenbauer, S. P. Harvey, D. E. Proffit and T. O. Mason, Transparent Conducting Oxides for Photovoltaics: Manipulation of Fermi Level, Work Function and Energy Band Alignment, *Materials*, 2010, **3**(11), 4892–4914, DOI: **10.3390/ma3114892**.

35 D. Lee, J. W. Park, N. K. Cho, J. Lee and Y. S. Kim, Verification of Charge Transfer in Metal-Insulator-Oxide Semiconductor Diodes via Defect Engineering of Insulator, *Sci. Rep.*, 2019, **9**, 10323, DOI: **10.1038/s41598-019-46752-1**.

36 Y. J. Tak, B. D. Ahn, S. P. Park, S. J. Kim, A. R. Song, K. B. Chung and H. J. Kim, Activation of sputter-processed indium-gallium-zinc oxide films by simultaneous ultraviolet and thermal treatments, *Sci. Rep.*, 2016, **6**, 21869, DOI: **10.1038/srep21869**.

37 Z. C. Zhuang, Y. Li, Z. L. Li, F. Lv, Z. Q. Lang, K. N. Zhao, L. Zhou, L. Moskaleva, S. J. Guo and L. Q. Mai, MoB/g-C3N4 Interface Materials as a Schottky Catalyst to Boost Hydrogen Evolution, *Angew. Chem., Int. Ed.*, 2018, **57**(2), 496–500, DOI: **10.1002/anie.201708748**.

38 B. C. Jang, Y. Nam, B. J. Koo, J. Choi, S. G. Im, S. H. K. Park and S. Y. Choi, Memristive Logic-in-Memory Integrated Circuits for Energy-Efficient Flexible Electronics, *Adv. Funct. Mater.*, 2018, **28**(2), 1704725, DOI: **10.1002/adfm.201704725**.

39 T. T. Trinh, K. Jang, S. Velumani, V. A. Dao and J. Yi, Role of Schottky barrier height at source/drain contact for electrical improvement in high carrier concentration amorphous InGaZnO thin film transistors, *Mater. Sci. Semicond. Process.*, 2015, **38**, 50–56, DOI: **10.1016/j.mssp.2015.03.051**.

40 M. Chun, J. G. Um, M. S. Park, M. D. H. Chowdhury and J. Jang, Effect of top gate potential on bias-stress for dual gate amorphous indium-gallium-zinc-oxide thin film transistor, *AIP Adv.*, 2016, **6**(7), 075217, DOI: **10.1063/1.4960014**.

41 R. Shvab, E. Hryha and L. Nyborg, Surface chemistry of the titanium powder studied by XPS using internal standard reference, *Powder Metall.*, 2017, **60**(1), 42–48, DOI: **10.1080/00325899.2016.1271092**.

42 S. Lee and D. C. Paine, Metallization selection and the performance of amorphous In-Zn-O thin film transistors,

Appl. Phys. Lett., 2014, **104**(25), 252103, DOI: **10.1063/1.4885118**.

43 S. Lee, K. Park and D. C. Paine, Metallization strategies for In2O3-based amorphous oxide semiconductor materials, *J. Mater. Res.*, 2012, **27**(17), 2299–2308, DOI: **10.1557/jmr.2012.141**.

44 J. Ka, E. N. Cho, M. J. Lee, J. M. Myoung and I. Yun, Electrode metal penetration of amorphous indium gallium zinc oxide semiconductor thin film transistors, *Curr. Appl. Phys.*, 2015, **15**(6), 675–678, DOI: **10.1016/j.cap.2015.03.004**.

45 C. I. Yang, T. C. Chang, P. Y. Liao, L. H. Chen, B. W. Chen, W. C. Chou, G. F. Chen, S. C. Lin, C. Y. Yeh, C. M. Tsai, M. C. Yu and S. D. Zhang, Drain-Induced-Barrier-Lowing-Like Effect Induced by Oxygen-Vacancy in Scaling-Down via-Contact Type Amorphous InGaZnO Thin-Film Transistors, *IEEE J. Electron Devices Soc.*, 2018, **6**(1), 685–690, DOI: **10.1109/Jeds.2018.2837682**.

46 D. H. Kim, K. H. Lee, S. H. Lee, J. Kim, J. Yang, J. Kim, S. I. Cho, K. H. Ji, C. S. Hwang and S. H. K. Park, Trench-Structured High-Current-Driving Aluminum-Doped Indium-Tin-Zinc Oxide Semiconductor Thin-Film Transistor, *IEEE Electron Device Lett.*, 2022, **43**(10), 1677–1680, DOI: **10.1109/Led.2022.3201072**.

47 H. J. Lee, C. H. Lee, N. T. Lian, M. C. Deng, T. H. Yang, K. C. Chen and C. Y. Lu, Effects of BCl3 gas on physical damage and Al residues in oxide hard-mask-based Al etching, *Semicond. Sci. Technol.*, 2007, **22**(6), 678–682, DOI: **10.1088/0268-1242/22/6/016**.

48 K. H. Lee, S. H. Lee, S. J. Cho, C. S. Hwang and S. H. K. Park, Improving the electrical performance of vertical thin-film transistor by engineering its back-channel interface, *Microelectron. Eng.*, 2022, **253**, 111676, DOI: **10.1016/j.mee.2021.111676**.

49 S. R. Thomas, P. Pattanasattayavong and T. D. Anthopoulos, Solution-processable metal oxide semiconductors for thin-film transistor applications, *Chem. Soc. Rev.*, 2013, **42**(16), 6910–6923, DOI: **10.1039/C3CS35402D**.

50 H. Bae, S. Kim, M. Bae, J. S. Shin, D. Kong, H. Jung, J. Jang, J. Lee, D. H. Kim and D. M. Kim, Extraction of Separated Source and Drain Resistances in Amorphous Indium–Gallium–Zinc Oxide TFTs Through C–V Characterization, *IEEE Electron Device Lett.*, 2011, **32**(6), 761–763, DOI: **10.1109/LED.2011.2127438**.