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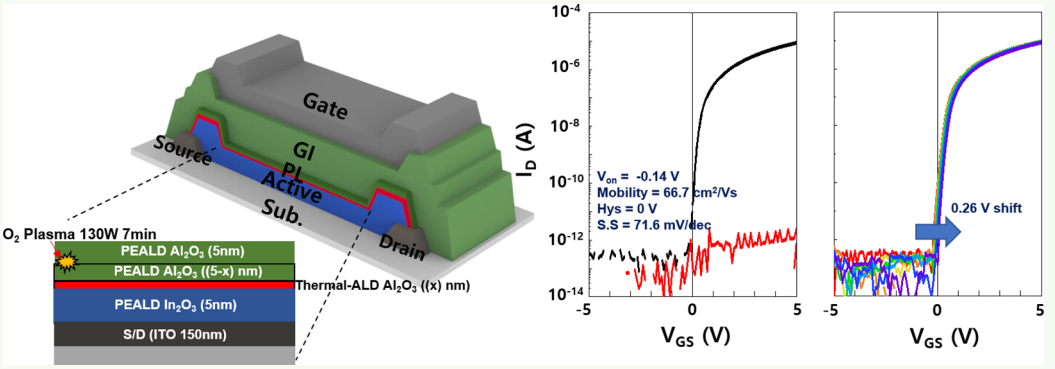
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Low-Thermal-Budget High-Mobility In_2O_3 Thin-Film Transistors Enabled by an In Situ Multifunctional Protection Layer

Sunghwan Park, Hwa Young Kim, Tae Hwan Boo, Hunbeom Shin, Seonghyun Kim, Seungbum Hong, and Sang-Hee Ko Park*

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ABSTRACT: While atomic layer deposition (ALD)-grown In_2O_3 thin-film transistors (TFTs) hold great promise for next-generation electronics, the performance and reliability of highly desirable top-gate configurations are often limited by interfacial degradation caused by photolithography chemicals and plasma exposure during device fabrication. Here, a multifunctional protection layer (PL) strategy is demonstrated that simultaneously suppresses chemical and plasma-induced interfacial damage while enabling controlled hydrogen incorporation. The introduction of an in situ plasma-free thermal ALD Al_2O_3 (T-Al_2O_3) layer directly onto the In_2O_3 channel, a robust physical barrier against chemical and plasma damage is established while simultaneously serving as a hydrogen reservoir. Crucially, inserting this T-Al_2O_3 layer allows for the precise tailoring of hydrogen incorporation by modulating the ALD cycles. The incorporated hydrogen effectively passivates interfacial defects, such as oxygen vacancies (V_O) and oxygen interstitials (O_i), while optimizing the carrier concentration. Consequently, the optimized top-gate TFTs deliver an exceptionally high field-effect mobility of 66.7 $cm^2/V{\cdot}s$, hysteresis-free operation, and outstanding operational stability, with a positive bias temperature stress (PBTS)-induced V_{on} shift of only 0.26 V and excellent resistance to negative-bias illumination stress (NBIS). Notably, these outstanding characteristics are achieved through a completely thermal annealing-free process. These results establish a powerful platform for simultaneous chemical and plasma damage suppression and hydrogen engineering in oxide semiconductor devices, enabling substantial improvements in both electrical performance and operational reliability.

KEYWORDS: *oxide semiconductors, thin-film transistors, atomic layer deposition, indium oxide, defect passivation, high mobility*

1. INTRODUCTION

Since the pioneering research by Hosono et al. in 2004, amorphous oxide semiconductors (OSs) have emerged as promising channel materials for thin-film transistors (TFTs).[1] Presently, the application of OSs is expanding well beyond conventional display backplanes, driving a major paradigm shift toward next-generation semiconductor technologies.[2−5] Their combination of relatively high mobility, ultra-low off-state current ($\leq 10^{-18}$ A/μm), and low-temperature process compatibility enables back-end-of-line (BEOL) integration with conventional CMOS platforms.[6−9] This renders them highly attractive for high-density memory such as DRAM and NAND flash, as well as logic, and image sensors.[4−6,10−13] For next-generation electronics, OS TFTs simultaneously achieve high mobility, low subthreshold swing (SS), near-zero turn-on voltage (V_{on}), low off-state leakage current, and high stability.[3,14,15] While representative materials include indium gallium zinc oxide (IGZO), indium tin zinc oxide (ITZO), and indium zinc oxide (IZO),

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simple binary oxides like indium oxide (In_2O_3) have recently garnered revitalized interest.[16−20] Among these, atomic layer deposition (ALD)-grown In_2O_3 offers distinct advantages. The self-limiting growth nature of ALD enables atomically smooth, ultrathin films, which effectively suppress surface roughness and carrier scattering.[21] Recent studies on ultrathin ALD grown In_2O_3 TFTs further highlight their potential as premier high-performance channel materials.[22−25] While the top-gate configuration is widely adopted for high-end TFT devices, it introduces critical fabrication challenges.[26−29] When the OS is directly exposed to chemical etchants during patterning, the surface suffers from severe defect generation and increased roughness, leading to substantial degradation of electrical characteristics.[30−33] To circumvent this chemical damage, a common strategy involves depositing a protection layer (PL) on the OS prior to simultaneous patterning.[30,34,35] However, a fundamental dilemma arises during the deposition of this PL. While plasma-enhanced ALD (PEALD) is highly preferred for depositing dense, high-quality dielectrics such as Al_2O_3, TiO_2, and HfO_2,[36−38] direct exposure to excessive plasma conditions severely damages the pristine GI/OS interface, which is particularly critical for achieving high performance and stability in oxide TFTs.[39,40] Such intense plasma exposures induce oxygen-related defect states and structural disorder at the GI/OS interface, which act as carrier trapping centers and ultimately degrade device performance and stability.[26,29,41,42] To improve carrier transport and reduce defect densities in both the bulk semiconductor and the GI/OS interface, many previously reported high-performance oxide TFTs rely on post-deposition high temperature thermal annealing.[42−44] However, such thermal treatments inevitably increase the process thermal budget and diminish the intrinsic advantages of oxide semiconductors for thermal sensitive platforms and BEOL-compatible electronics.[25,45] Although post-fabrication annealing and plasma process optimization can partially mitigate these issues, neither approach can fully prevent plasma-induced interfacial degradation. Recent efforts have utilized a sacrificial Thermal ALD Al_2O_3 (T-Al_2O_3) overlayer to block plasma-induced defect generation at the GI/OS interface.[46] However, the necessity of etching this plasma shielding layer introduces undesirable process complexity and completely discards its inherently high hydrogen content. Given that moderate hydrogen incorporation is well known to enhance device performance by increasing free electron concentration and mobility, while simultaneously passivating defects at the GI/OS interface such as oxygen vacancies (V_O) and oxygen interstitials (O_i) to improve positive bias temperature stress (PBTS) stability,[26,41,47−49] removing this hydrogen-rich layer fundamentally limits the overall potential of the TFTs. To overcome these critical limitations, herein we propose a multifunctional PL strategy that simultaneously suppresses chemical damage and plasma-induced interfacial damage while enabling controlled hydrogen incorporation. Specifically, we integrated an in-situ plasma-free T-Al_2O_3 layer immediately following the In_2O_3 channel deposition. The employment of this ultrathin T-Al_2O_3 PL provides several distinct advantages. First, it serves as a robust physical barrier, mitigating the chemical damage introduced during the subsequent patterning process. Second, it effectively shields the pristine channel interface from severe plasma-induced degradation during the subsequent PEALD GI deposition. Third, because the T-Al_2O_3 process utilizes H_2O as a reactant, the as-deposited layer inherently possesses a higher hydrogen concentration. By preserving this layer rather than etching it away, we enable highly effective hydrogen incorporation into the channel region, which passivates interfacial traps and significantly enhances the electrical characteristics. However, excessive hydrogen can render the TFT overly conductive, causing a negative V_{on} shift and aggravating PBTS-induced degradation.[26,29,50] To balance this delicate trade-off, we tailored the extent of hydrogen incorporation by precisely controlling the T-Al_2O_3 thickness via the number of ALD cycles. Previous work demonstrated hydrogen engineering in In_2O_3 TFTs using ALD-based super-cycle strategies.[51] In contrast, the present approach employs a localized ultrathin T-Al_2O_3 layer within the multifunctional PL to mitigate process-induced interfacial damage while enabling controlled hydrogen incorporation without post-fabrication thermal annealing. Detailed analytical studies, including X-ray photoelectron spectroscopy (XPS) and secondary ion mass spectrometry (SIMS), verify that the multifunctional PL architecture effectively passivates plasma-induced interfacial defects while enabling the precise control of hydrogen incorporation. Consequently, the optimized top-gate TFTs demonstrated outstanding performance, achieving an exceptionally high field-effect mobility of 66.7 $cm^2/V{\cdot}s$ alongside remarkable operational stability with a negligible PBTS V_{on} shift of merely 0.26 V. Notably, achieving these results without any thermal annealing represents a significant advancement, as it enables compatibility with BEOL processes and thermally sensitive platforms. These results establish a viable pathway for simultaneously mitigating plasma-induced interfacial damage and engineering hydrogen incorporation in oxide semiconductor devices.

2. EXPERIMENTAL SECTION

The overall fabrication procedure is illustrated in Figure 1. Top-gate bottom-contact (TGBC) TFTs were fabricated on glass substrates via a sequential deposition protocol to investigate the effects of PL insertion on chemical damage suppression, plasma shielding, and hydrogen incorporation. First, a 150-nm-thick ITO layer was deposited to act as the source/drain electrodes. Subsequently, a 5-nm-thick In_2O_3 active channel was grown at 200 °C under a chamber pressure below 1 Torr using a PEALD process. The PEALD process employed [3-(dimethylamino) propyl] dimethylindium (DADI), maintained at 40 °C in a precursor canister, as the indium source, alongside a 100 W radio-frequency (RF) O_2 plasma as the reactant. A single deposition cycle consisted of the following four consecutive steps: (1) introduction of the DADI precursor for 1.0 s using an Ar carrier gas flow of 50 sccm, (2) chamber purging with Ar for 10 s, (3) exposure to the 100 W RF O_2 plasma for 2.0 s at an O_2 flow rate of 500 sccm, and (4) a final Ar purge for 10 s.

2.1. PL Formation

After the deposition of the 5-nm-thick In_2O_3 channel, a 10-nm-thick Al_2O_3 PL was deposited in situ within the same ALD chamber without breaking vacuum to afford chemical protection during the subsequent patterning processes, while simultaneously serving as a plasma shield and enabling hydrogen incorporation. The PL consisted of a bottom 5-nm engineered layer comprising T-Al_2O_3 (x nm)/PEALD Al_2O_3 ($5 - x$ nm), followed by an additional 5-nm PEALD Al_2O_3 layer. To systematically investigate the protective and passivation effects, various PL architectures were designed by varying the T-Al_2O_3 thickness (x = 0, 0.25, 0.5, and 0.75-nm) and selectively applying the intermediate O_2 plasma treatment, as schematically illustrated in Figure 2a-e and detailed in Table 1. During the T-Al_2O_3 process, both TMA and H_2O precursors were maintained at ambient temperature, and the deposition was conducted under a chamber pressure below 1 Torr.

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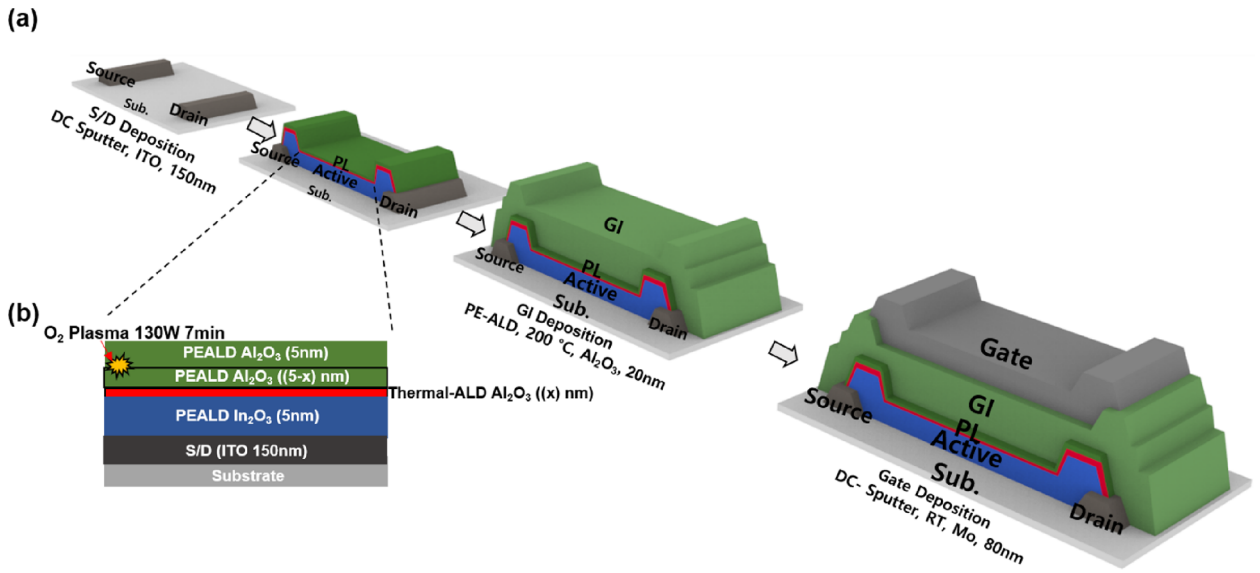


Figure 1. (a) Schematic illustration of the fabrication procedure and the detailed structural architecture of the TGBC In_2O_3 TFTs. (b) Architecture details the 10-nm PL stack: T-Al_2O_3 (x nm) / PEALD Al_2O_3 ((5−x) nm) bilayer, followed by an intermediate O_2 plasma treatment and a 5-nm PEALD Al_2O_3 layer.

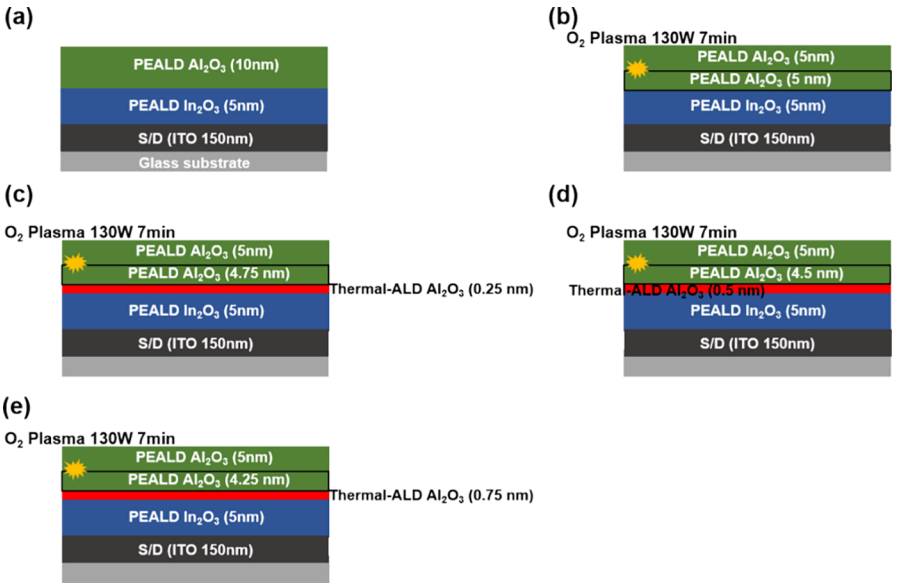


Figure 2. Structural variations of the 10-nm PL stack applied to the In_2O_3 TFTs. Schematics of the control devices (a) without and (b) with the intermediate O_2 plasma treatment. The engineered PL stacks comprising a T-Al_2O_3 (x nm) / PEALD Al_2O_3 ((5−x) nm) bottom layer, O_2 plasma treatment, and 5-nm PEALD Al_2O_3 top layer, with x varied as (c) 0.25, (d) 0.5, and (e) 0.75.

Table 1. Detailed Layer Thicknesses and Fabrication Conditions of the Engineered 10-nm PL Stacks Applied to the In_2O_3 TFTs

structure illustrate of PL	thickness of T-Al_2O_3 [nm]	thickness of PE-Al_2O_3 bilayer [nm]	intermediate O_2 plasma treatment	thickness of PE-Al_2O_3 top layer [nm]
Figure 2a	0	5	X	5
Figure 2b	0	5	130 W 7 min	5
Figure 2c	0.25	4.75	130 W 7 min	5
Figure 2d	0.5	4.5	130 W 7 min	5
Figure 2e	0.75	4.25	130 W 7 min	5

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T-Al_2O_3 deposition cycle was defined by the following steps: (1) 0.2 s TMA dose with 500 sccm Ar, (2) 5.0 s Ar purge, (3) 0.3 s H_2O dose with 500 sccm Ar, and (4) 7.0 s Ar purge. Subsequently, an O_2 plasma treatment (130 W, 7 min) was applied to this intermediate stack to regulate oxygen-related bulk defects.[51] The final 5-nm-thick PEALD Al_2O_3 layer was then deposited to complete the PL. Following the simultaneous patterning of the PL and active layer, a main GI of 20-nm-thick PEALD Al_2O_3 was deposited, bringing the total effective GI thickness to 30-nm. For all PEALD Al_2O_3 deposition steps, a unified cycle was employed: (1) 0.2 s TMA dose with 500 sccm Ar, (2) 5.0 s Ar purge, (3) 2.0 s RF O_2 plasma exposure at 60 W with 500 sccm O_2, and (4) 7.0 s Ar purge.

Following the dielectric deposition, the fabrication was concluded with the formation of contact vias and the DC-sputtering of an 80-nm-thick Mo gate electrode at room temperature. All patterning was performed using photolithography and wet chemical etching. The completed devices featured channel widths (W) and lengths (L) of 40 and 20 μm, respectively. Cross-sectional TEM and EDS analyses were performed on the completed devices to verify the device structure and elemental distribution across the stacked layers. (Figure S1, Supporting Information)

Electrical characteristics and bias stability parameters were extracted at room temperature in complete darkness to suppress unintended light-induced phenomena. These measurements utilized a probe station integrated with an HP 4156A parameter analyzer and an Agilent 4284A LCR meter. To ensure statistical consistency, 10 independent samples per condition were measured. The thicknesses of the deposited films were verified by spectroscopic ellipsometry (ALPHA-SE). Additionally, to enable a comparative analysis of hydrogen incorporation within the varied PL configurations. X-ray photoelectron spectroscopy (XPS, Thermo Scientific K-Alpha+) and secondary ion mass spectrometry (SIMS, CAMECA IMS-7f) measurements were conducted on samples that exactly mirrored the TFT deposition processes.

3. RESULT AND DISCUSSION

To visually evaluate the chemical shielding efficacy of the multifunctional PL, the surface morphologies were characterized using atomic force microscopy (AFM) before and after the simulated photolithography process (Figure 3). The pristine In_2O_3 exhibited an atomically smooth surface with a root-mean-square (RMS) roughness of 0.161 nm (Figure 3a). However, after exposure to the harsh patterning chemicals (developer, etchant, and stripper), the pristine surface was severely degraded, resulting in an increased RMS roughness of 0.327 nm (Figure 3b),

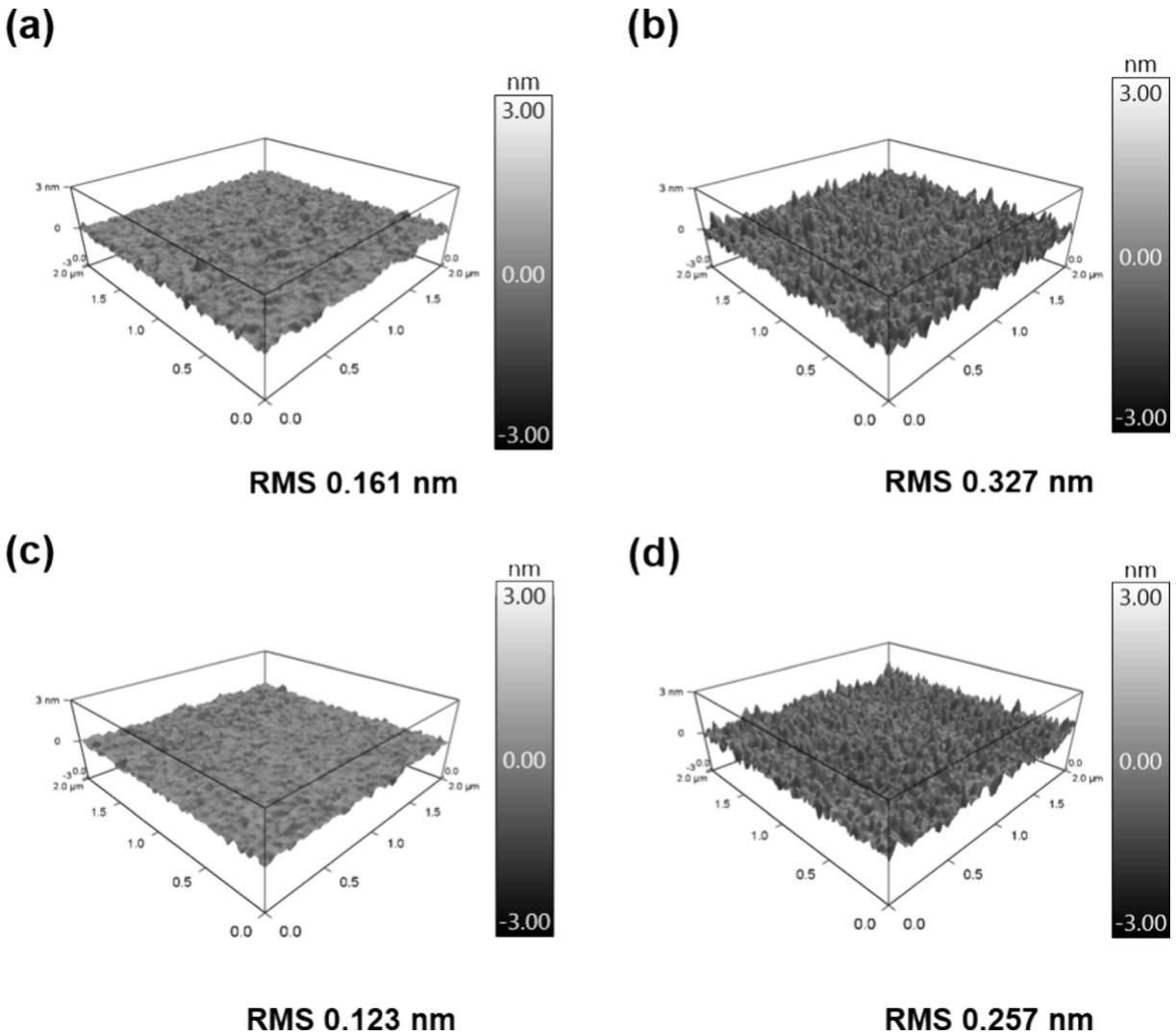


Figure 3. AFM surface images of (a) pristine In_2O_3, (b) In_2O_3 after exposure to photolithography chemicals, (c) pristine PL-covered In_2O_3, and (d) PL-covered In_2O_3 after identical chemical exposure.

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which indicates direct chemical damage to the active channel. As extensively reported in previous studies, such direct exposure and subsequent roughening of oxide semiconductor surfaces can induce additional interfacial trap states, potentially deteriorating the electrical performance of top-gate OS TFTs.[30−33]

A similar morphological alteration was observed in the PL-covered sample, where the RMS roughness increased from 0.123 nm (Figure 3c) to 0.257 nm (Figure 3d) following the identical chemical exposure. Importantly, Figure 3d characterizes the exposed top surface of the PL, where the increase in RMS roughness indicates morphological modification induced by the chemical treatment. In the proposed device architecture, the 10-nm PL serves as a physical shielding layer that separates the underlying In_2O_3 channel from direct contact with the patterning chemicals, thereby reducing its chemical exposure.

As illustrated in Figure 4, the fabricated TGBC TFT devices display distinct electrical trends depending on the T-Al_2O_3 thickness within the PL. To evaluate the linear-region transfer characteristics, a drain voltage (V_d) of 0.1 V was applied to the TFTs (W/L = 40/20 μm), with solid and dashed lines denoting the forward and reverse sweeps, respectively. Field-effect mobility was calculated at V_d = 0.1 V based on the respective V_{on} and the experimentally determined gate insulator capacitance (C_i) for each PL configuration (Figure S2). Since Metal-Insulator-Metal (MIM) measurements confirmed a uniform capacitance of ∼0.26 μF/cm^2 across all five 30-nm-thick Al_2O_3 gate insulators, the observed fluctuations in V_{on} among the fabricated devices can likely be attributed to variations in carrier concentrations and defect states. Furthermore, the output characteristics of all fabricated TFTs, presented in Figure S3, verify the onset of current saturation and demonstrate robust saturation behavior with increasing V_{DS}. The nearly linear behavior in the low-V_{DS} region indicates ohmic-like carrier injection at the S/D contacts. *Y*-function analysis further revealed a slight decrease in contact resistance with increasing T-Al_2O_3 thickness within the PL.[52] However, the relatively modest variation suggests that contact resistance is unlikely to be a primary contributor to the enhanced electrical performance. (Figure S4) Additionally, based on the analysis of transfer characteristics across different T-Al_2O_3 thicknesses within the PL, the extracted average electrical parameters for 10 devices are summarized in Table 2.

During the PL process, increasing the T-Al_2O_3 thickness from 0 to 0.75-nm was associated with enhanced hydrogen

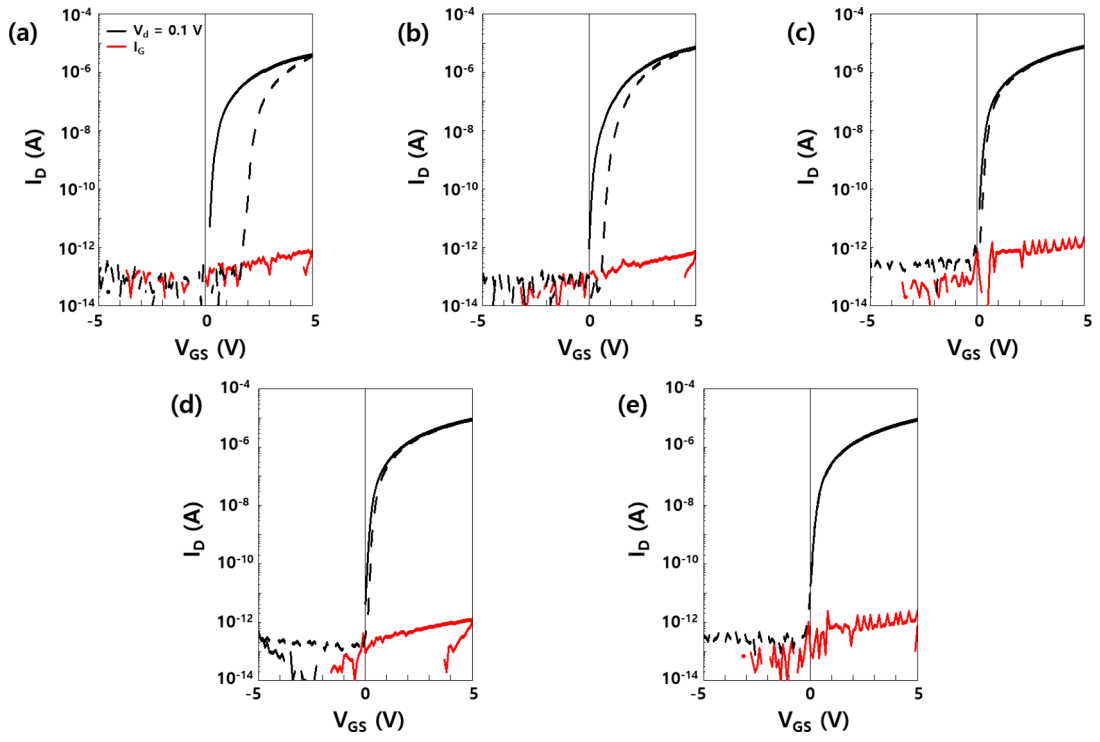


Figure 4. Transfer characteristics of TFTs with different PL configurations: (a) 0 nm T-Al_2O_3 without O_2 plasma treatment, and (b−e) with intermediate O_2 plasma treatment and T-Al_2O_3 thicknesses of (b) 0 nm, (c) 0.25 nm, (d) 0.5 nm, and (e) 0.75 nm within the PL.

Table 2. Extracted Electrical Parameters (at V_d = 0.1 V) with Average and Standard Deviation Obtained from Measurements On 10 Devices With Different Thickness of T-Al_2O_3

thickness of T-Al_2O_3 [nm]	V_{on} [V]	μ_{lin} [cm^2/Vs]	S.S [mV/dec]	Hysteresis [V]
0 (w/o O_2 PT)	0.25 ± 0.085	32.07 ± 2.63	76.5 ± 8.0	1.53 ± 0.16
0 (with O_2 PT)	0.03 ± 0.05	53.99 ± 1.57	74.7 ± 7.5	0.65 ± 0.09
0.25	0.01 ± 0.03	54.19 ± 2.08	72.4 ± 9.2	0.19 ± 0.06
0.5	0.01 ± 0.03	63.27 ± 0.38	71.6 ± 4.2	0.14 ± 0.03
0.75	−0.14 ± 0.05	66.70 ± 0.44	71.6 ± 3.4	0

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incorporation, which can contribute to donor formation. Correspondingly, the linear field-effect mobility (μ_{lin}) was significantly enhanced, increasing from 53.99 to 66.7 cm^2 V^{-1} s^{-1}. The fundamental mechanism driving this mobility improvement can be understood by examining the relationship between V_{on} and the PL-deposited T-Al_2O_3 thickness. The H_2O-based thermal ALD process used for T-Al_2O_3 provides a plausible pathway for hydrogen incorporation, which can function as both a shallow donor and a defect passivator in the OS.[26,41,47,49,51] These combined roles enhance the device mobility through two mechanisms: first, by donating electrons to increase the carrier amounts, which activates the percolation conduction typical of OSs and second, by passivating electron trap states, which reduces the potential barriers to electron transport and thereby improves the overall conductivity. Concurrently, this mobility improvement is accompanied by a negative shift in the V_{on} from 0.03 to −0.14 V, illustrating a clear trade-off between enhanced carrier transport and elevated donor concentration. Typically, an increase in carrier concentration drives V_{on} toward more negative values. Critically, when the T-Al_2O_3 thickness reaches 2-nm, excessive hydrogen incorporation makes the device entirely conductive, resulting in a complete loss of switching behavior, as depicted in Figure S5a. Moreover, an increased T-Al_2O_3 thickness within the PL provides enhanced protection for the OS channel against plasma-induced damage during subsequent processing steps.[46] Concurrently, the hydrogen incorporated from the PL contributes to the passivation of charge-trapping sites located at the GI/OS interface and within the bulk GI. Because charge trapping during forward and reverse V_G sweeps alters the overall current−voltage characteristics and gives rise to hysteresis, this hydrogen-mediated defect passivation significantly suppresses device hysteresis. Remarkably, increasing the T-Al_2O_3 thickness from 0 to 0.75-nm during the PL process suppressed this hysteresis, reducing it from 0.65 V to 0 V. This remarkable enhancement in operational stability strongly suggests that the incorporated hydrogen passivates the active trap states. Specifically, the comparative analysis between the control devices without (Figure 4a) and with (Figure 4b) the O_2 plasma treatment shows that the O_2 plasma treatment significantly suppresses hysteresis and improves device mobility. Furthermore, even the device incorporating the optimized T-Al_2O_3 thickness of 0.75 nm exhibits inferior performance when the O_2 plasma treatment is omitted, displaying a residual hysteresis of 1.1 V and a reduced mobility of ∼45 $cm^2V^{-1}s^{-1}$ (Figure S5b). These results highlight the important contribution of the intermediate O_2 plasma treatment to achieving the optimized electrical characteristics. Furthermore, a comparison between the 0-nm T-Al_2O_3 devices (Figure 4b) and the device with 0.25-nm of T-Al_2O_3 within the PL (Figure 4c) reveals a significant reduction in hysteresis in the latter, despite both exhibiting nearly identical mobilities. This improvement can be attributed to the introduction of the 0.25-nm-thick T-Al_2O_3 layer, which not only mitigates interfacial defects by partially shielding the channel from plasma-induced damage during PEALD, but also supplies hydrogen that functions predominantly as a defect passivator rather than a shallow donor. Although the T-Al_2O_3 thickness within the PL was increased by only a few atomic layers, the device characteristics underwent significant modulation. Specifically, the optimal T-Al_2O_3 thickness of 0.75-nm yielded outstanding electrical properties, including an exceptional mobility of 66.7 cm^2 V^{-1} s^{-1}, well-balanced SS and V_{on} parameters, and completely suppressed hysteresis.

The value of μ_{lin} is calculated using

$$\mu_{lin} = \frac{g_m}{\frac{W}{L}\cdot C_i \cdot V_d} \qquad \left(\text{where } g_m \equiv \frac{\partial I_d}{\partial V_g}\right)$$

The SS was extracted from the transfer characteristics using the following equation:[53]

$$SS = \left(\frac{d\log(I_{DS})}{dV_{GS}}\right)^{-1}$$

In addition, the value of V_{on} was calculated using

$$V_{on} = V_G \qquad \left(\text{where } I_D = 10pA \times \frac{W}{L}\right)$$

where W and L denote the channel width and length, respectively, and the GI parameters, including C_i and the dielectric constant (k), are detailed in Figure S2.

To verify that introducing a T-Al_2O_3 layer at the GI/OS interface within the PL enables precise control over hydrogen-related components, SIMS analysis was employed. Because the T-Al_2O_3 layer was deposited using H_2O as the reactant, it can provide a plausible source of hydrogen-containing species and the subsequent GI deposition process at 200 °C provides a thermal environment that can hydrogen diffusion from the T-Al_2O_3 layer toward the adjacent In_2O_3 channel region.[54] In OSs, hydrogen can exist in various chemical configurations, including interstitial hydrogen, hydrogen bonded to oxygen or metal atoms, hydrogen residing at V_O defects, and hydroxyl-related species.[41,55,56] Although SIMS does not directly distinguish the exact chemical state of hydrogen, it provides valuable information regarding the relative distribution of hydrogen-related species throughout the film stack. Consequently, hydrogen and hydroxyl (OH) depth profiles were investigated, as these species are known to function as both electron donors and defect passivators in OSs.[26,41,47,51,56] As depicted in Figure 5a,b, the depth profiles of hydrogen and OH species were measured in film samples with the identical stack sequence as the fabricated top-gate devices.

As the T-Al_2O_3 thickness within the PL increased, the hydrogen-related signals in the channel region adjacent to the GI/OS interface generally increased, indicating enhanced hydrogen incorporation associated with the H_2O-based T-Al_2O_3 process (Figure 5a). Interestingly, however, the 0.25-nm T-Al_2O_3 device exhibited a slightly lower hydrogen intensity than the 0-nm T-Al_2O_3 device, despite showing a significantly enhanced OH signal. This inverse trend between the hydrogen and OH signals suggests a change in the local chemical environment of the incorporated hydrogen. Rather than remaining as highly mobile hydrogen species, a portion of the incorporated hydrogen is likely converted into hydroxyl-related configurations through interactions with V_O defects or weakly bonded oxygen.[26,41,55] Such a tendency is consistent with the transfer characteristics (Figure 4b,c), where the field-effect mobility remained nearly constant at ∼54 cm^2 $V^{-1}s^{-1}$ even after introducing the 0.25-nm T-Al_2O_3 layer, showing minimal deviation from the 0-nm T-Al_2O_3 device. This effective defect passivation, however, significantly enhanced the overall device stability. The hysteresis decreased from 0.65 to 0.19 V, and the V_{on} shift was remarkably reduced from 2.04 to 1.23 V, a trend that will be

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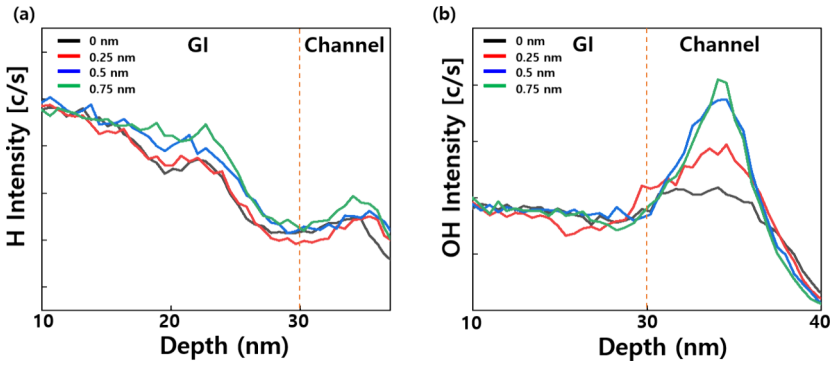


Figure 5. SIMS depth profiles of (a) H and (b) OH in the GI/active/substrate structure with varying T-Al_2O_3 thicknesses (0, 0.25, 0.5, and 0.75 nm) within the PL.

further corroborated by the PBTS stability analyses discussed in the subsequent section.

As depicted in Figure 5b, the OH intensities exhibit a clear and consistent trend. Specifically, the OH intensity within the channel layer increases proportionally with the T-Al_2O_3 thickness in the PL. The 0-nm T-Al_2O_3 device exhibited the lowest OH intensity, which gradually increased for the 0.25 and 0.5-nm T-Al_2O_3 devices, ultimately reaching the highest intensity in the 0.75-nm T-Al_2O_3 device. Consistent with the dual role of hydrogen discussed above, this progressively increased OH signal is well correlated with the electrical characteristics shown in Figure 4. As the T-Al_2O_3 thickness increased from 0.25 to 0.75-nm, the field-effect mobility continuously improved from 54.19 to 66.7 $cm^2\ V^{-1}\ s^{-1}$, accompanied by a gradual negative shift in V_{on}. These observations suggest that the incorporated hydrogen simultaneously participates in both defect passivation and carrier generation. The progressively increased OH signal further indicates that a portion of the incorporated hydrogen forms hydroxyl-related configurations. Hydrogen incorporation has also been reported to contribute to shallow donor formation through interactions with weakly bonded lattice oxygen(O^{2-}), described by $H_i^+ + O^{2-} \rightarrow OH^- + e^-$.[55,57] This process provides a plausible explanation for the concurrent increase in OH-related species and carrier concentration, while hydrogen interactions with oxygen-related defects, including both V_O and O_i states, contribute to defect passivation.[26,41,49,55] At relatively low hydrogen concentrations, the electrical impact of donor-generated carriers may be effectively compensated by the remaining trap states, making defect passivation the dominant observable effect. As hydrogen incorporation increases, its role as a shallow donor becomes increasingly evident. Such hydrogen incorporation may facilitate percolation conduction within the In_2O_3 channel, thereby contributing to the observed mobility enhancement. As reflected by the pronounced performance variations observed in this study, even trace amounts of hydrogen can profoundly influence the electrical properties of high-mobility OSs, particularly in materials with high intrinsic carrier densities.

To investigate the effect of hydrogen incorporation driven by varying the T-Al_2O_3 thickness within the PL on the oxygen bonding states at the GI/In_2O_3 interface, depth profile XPS O1s analysis was conducted on the stacked films (Figure 6). To accurately replicate the practical device architecture, the analyzed film samples were prepared following the identical TGBC process flow. This analysis is essential because the characteristics of OSs are strongly affected by their oxygen binding states.[58] The O1s spectra were deconvoluted into three primary fractions corresponding to metal−oxygen (M−O) bonds (530.4 ± 0.1 eV), oxygen vacancies (V_O, 531.4 ± 0.1 eV), and metal−hydroxyl (M−OH) groups (532.5 ± 0.1 eV).[26,29] The relative proportions of the distinct oxygen chemical states were quantified by integrating the areas of their respective deconvoluted sub-peaks. As shown in Figure 6a,b, when comparing the devices without T-Al_2O_3 layer (0-nm), the only fabrication difference is the application of the O_2 plasma treatment to the bulk Al_2O_3 within the PL. Consequently, both devices exhibit nearly identical interfacial O 1s components (M−O, V_O, and M−OH), indicating that the bulk O_2 plasma treatment alone does not significantly alter the chemical states at the GI/OS interface. In contrast, the O 1s spectra of the bulk region within the PL for the 0-nm T-Al_2O_3 devices (Figure S6) reveal that the O_2 plasma treatment applied to the bulk Al_2O_3 increased the Al−O-related component while decreasing the component assigned to V_O-related states. These results indicate that the O_2 plasma treatment modifies the oxygen-related chemical states within the bulk PL, which may contribute to the reduced charge trapping and suppressed hysteresis observed in the electrical characteristics.

Regarding the GI/OS interface for devices with T-Al_2O_3 thicknesses ranging from 0 to 0.75-nm (Figure 6b−e), significant compositional variations are observed. As previously discussed, aggressive O_2 plasma processes during the GI deposition inherently generate oxygen-related interfacial defect states that act as electron-trapping centers, thereby inducing charge trapping and device instability. As the T-Al_2O_3 thickness within the PL increased, the improved shielding against plasma-induced damage and enhanced hydrogen incorporation were accompanied by progressive modification of the interfacial defect chemistry. Previous studies have suggested that incorporated hydrogen can interact with O_i defects, leading to the formation of hydroxyl species and defect passivation.[55,59] Such hydrogen-mediated interactions are expected to suppress electron-trapping centers at the GI/OS interface. Consequently, the OH fraction increased from 4.85% to 10.12% with increasing T-Al_2O_3 thickness. Consistent with the SIMS results depicted in Figure 5b, the increased OH fraction indicates enhanced incorporation of hydrogen-related species at the GI/OS interface which is associated with the passivation of oxygen-related defects. Specifically, the relative fraction of the V_O-related component exhibited a decreasing trend from 34.54% to 26.58%. The reduction in the V_O-related fraction is consistent with the

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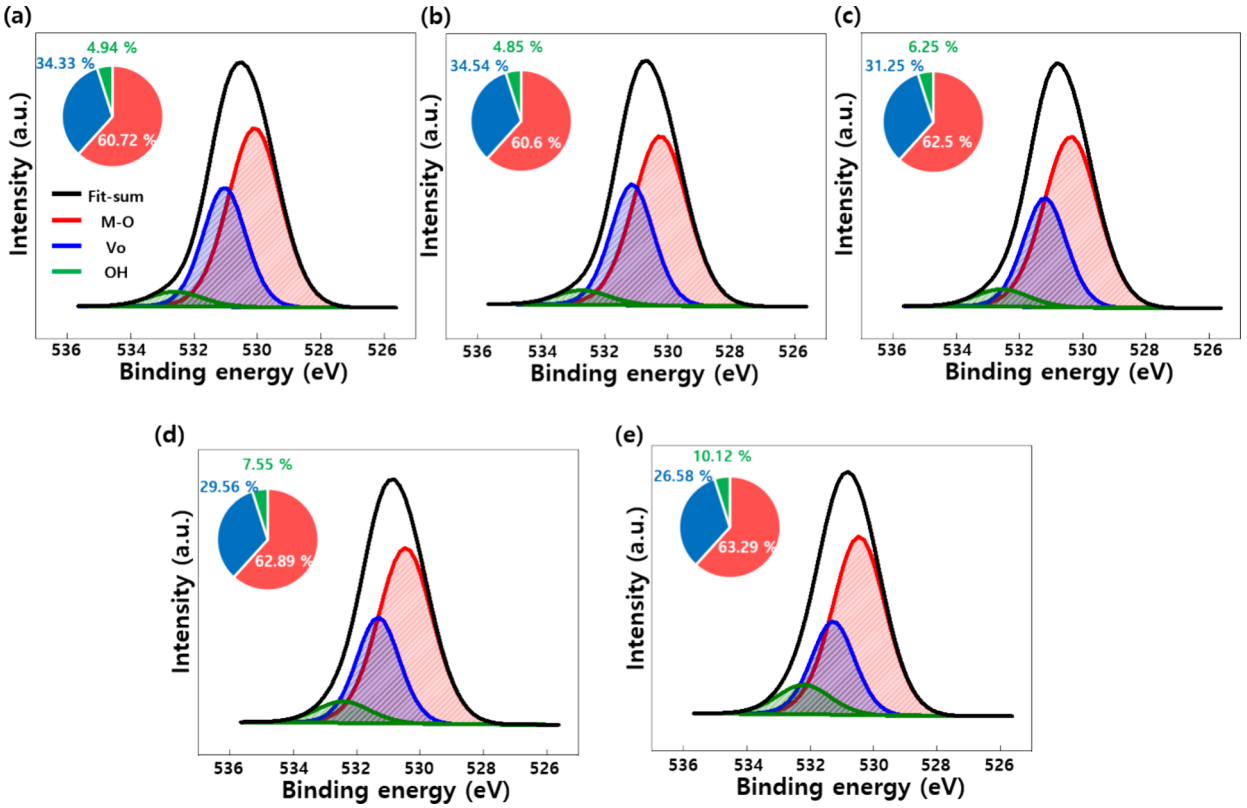


Figure 6. XPS O 1s spectra of the GI/In_2O_3 interface for the control devices (a) without and (b) with O_2 plasma (0-nm T-Al_2O_3), and for the engineered PL stacks with varying T-Al_2O_3 thicknesses of (c) 0.25, (d) 0.5, and (e) 0.75-nm.

hydrogen-passivation mechanism reported in previous studies, which can be described as: $H_i^+ + V_O \rightarrow H_O^+$.[51,55] The observed compositional evolution, specifically the simultaneous decrease in the V_O-related fraction and increase in the OH fraction, is further corroborated by the SIMS depth-profile trends, suggesting hydrogen-mediated modification of oxygen-related defect states at the interface. These compositional changes are well correlated with the improved electrical characteristics, including enhanced mobility and reduced hysteresis. Furthermore, as will be detailed in the following section, these changes contribute to improved bias-stress stability. Therefore, these final-state chemical results, together with the SIMS and electrical characteristics, support the role of controlled hydrogen incorporation associated with the T-Al_2O_3 layer in optimizing both the interfacial defect chemistry and device performance. Moreover, the GI/OS interface trap density (D_{it}) was extracted via the following equation to corroborate the trap reduction:

$$D_{it} = \frac{C_i}{q} \cdot \left(\frac{S.S}{(\ln 10) kT/q} - 1 \right)$$

where kT is the thermal energy and q is the elementary charge. The extracted D_{it} values exhibit a decreasing trend with increasing the T-Al_2O_3 thickness within the PL.[53,60−62] Specifically, 3.81×10^{11}, 3.26×10^{11}, 3.07×10^{11}, and 3.04×10^{11} $cm^{-2}{\cdot}eV^{-1}$ for for 0, 0.25, 0.5, and 0.75-nm T-Al_2O_3 within the PL, respectively. This decrease aligns well with the defect passivation corroborated by the hysteresis, XPS, and SIMS measurements. As it is extracted via the SS method, this effective D_{it} serves as a supplementary parameter that comprehensively reflects the overall trend of defect passivation.

To further substantiate the enhanced hydrogen incorporation and its effect on the defect states at the GI/OS interface for devices with T-Al_2O_3 thicknesses increasing from 0 to 0.75-nm, metal−insulator−semiconductor (MIS) capacitance−voltage (C−V) measurements were performed. These measurements were carried out at a high frequency of 1 MHz and at room temperature (295 K) to minimize the response of slow interfacial trap states and other slow charge-trapping processes.[63] Under these high-frequency conditions, the hysteresis voltage (ΔV_{Hys}) is directly proportional to the trapped charge density ($Q_{trapped}$), and therefore serves as a useful indicator of defect passivation.[63] The trapped charge density can be estimated using the following relation:

$$Q_{trapped} = C_{OX} \times \Delta V_{Hys} \times \frac{1}{q}$$

where C_{ox} is the oxide capacitance per unit area and q is the elementary charge. Given that q is a constant and C_{ox} remains nearly identical across all devices, as confirmed in Figure S2, a smaller ΔV_{Hys} corresponds to a lower density of trapped charge and more effective defect passivation. As illustrated in Figure 7a−d, ΔV_{Hys} systematically decreases as the thickness of the T-Al_2O_3 layer within the PL increases. This progressive narrowing of the hysteresis window indicates the systematic suppression of charge trapping, supporting the proposed mechanism of defect passivation by hydrogen incorporation. These

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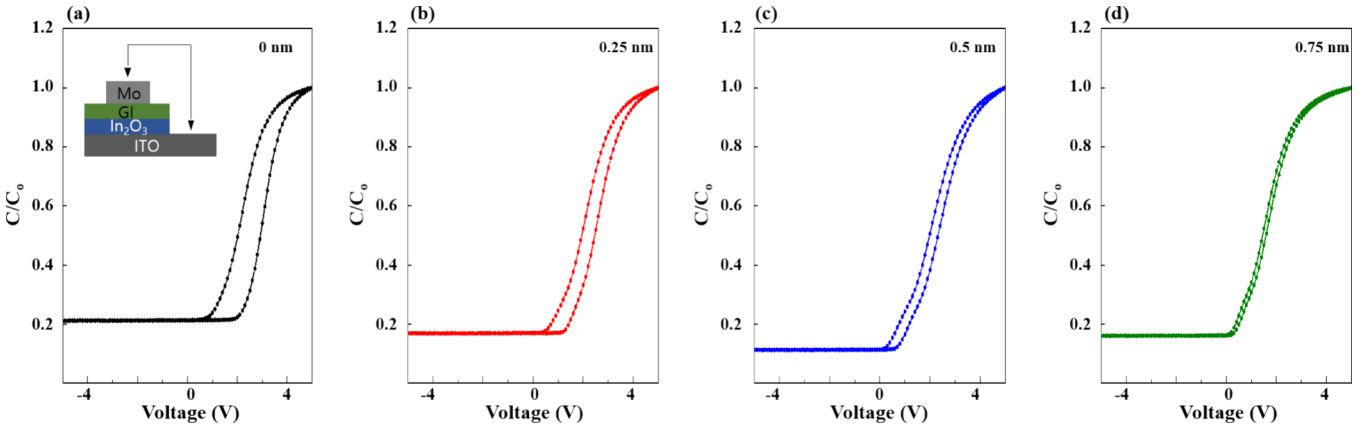


Figure 7. *C*−*V* characteristics of MIS capacitors with varying T-Al_2O_3 thicknesses (a) 0 nm, (b) 0.25 nm, (c) 0.5 nm and (d) 0.75 nm.

results are highly consistent with the XPS analysis at the GI/OS interface, which revealed a decrease in the relative fraction of the V_O-related component together with an increase in OH content. However, for comparison, the device without the T-Al_2O_3 layer (0-nm) and without the O_2 plasma treatment exhibited a significantly larger ΔV_{Hys}, as depicted in Figure S7, further highlighting the effectiveness of the proposed protection-layer engineering approach.

To further evaluate the overall charge-trapping behavior beyond the *C*−*V* hysteresis analysis, the flat-band voltage shift (ΔV_{FB}) was also examined. In OSs, the flat-band voltage shift (ΔV_{FB}) can reflect the cumulative effects of interface and bulk traps and fixed charges.[64] To accurately quantify this, ΔV_{FB} was extracted using the inflection point method, defined by the maximum peak of the first derivative (dC/dV) corresponding to the zero-crossing of the second derivative.[65,66] (Figure S8) A monotonic reduction in ΔV_{FB} was observed with increasing T-Al_2O_3 thickness. This systematic suppression of ΔV_{FB} indicates that increasing the T-Al_2O_3 layer thickness within the PL effectively mitigates charge trapping associated with the GI/OS interface and the bulk GI. Notably, for the 0-nm T-Al_2O_3 devices, applying O_2 plasma treatment to the bulk PL reduced ΔV_{FB} (Figure S9), consistent with reduced bulk-dielectric-related charge trapping and the corresponding suppression of transfer hysteresis (Table 2).

In conventional PBTS theory, electron trapping within the GI or at the GI/OS interface, associated with defects such as V_O, O_i, and dangling bonds, has been widely accepted as the primary degradation mechanism responsible for positive V_{on} shifts.[15,67,68] Additionally, the intrinsic defects in In_2O_3 can negatively affect the stability of TFTs.[51] These defects act as charge trapping centers, which capture accumulated carriers and lead to device instability. The extent of the V_{on} shift is directly proportional to the frequency of charge trapping at these sites. This correlation highlights the critical role of defect passivation in improving the PBTS stability and overall device reliability. PBTS stability tests were performed under a bias condition of 1 MV/cm at 60 °C for 3600 s, the transfer curves illustrating V_{on} shifts for each device are depicted in Figure 8.

As shown in Figure 8a,b, the sole fabrication difference between the two 0-nm T-Al_2O_3 devices lies in the O_2 plasma treatment applied to the bulk Al_2O_3 within the PL. Without this treatment, the device exhibited a substantial V_{on} shift of 2.40 V. Conversely, the application of the O_2 plasma treatment to the bulk Al_2O_3 reduced the V_{on} shift to 2.04 V. This reduction suggests that O_2 plasma treatment modifies the charge-trapping environment within the bulk PL, consistent with the changes in bulk dielectric chemical states observed by XPS analysis (Figure S6). Such modification of bulk dielectric defect states can influence charge trapping under positive bias. As illustrated in Figure 8c−e, increasing the T-Al_2O_3 thickness within the PL resulted in a systematic reduction in the positive V_{on} shift. The V_{on} shift was restricted to 1.23 V for the 0.25-nm T-Al_2O_3 device and 0.90 V for the 0.5-nm T-Al_2O_3 device. Remarkably, the device with the 0.75-nm T-Al_2O_3 layer demonstrated an exceptionally small V_{on} shift of 0.26 V, indicating a

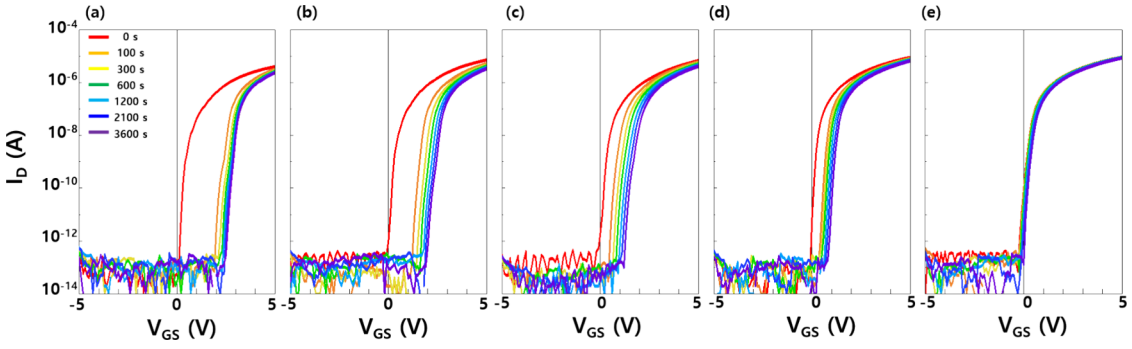


Figure 8. Evolution of the transfer characteristics of In_2O_3 TFTs during PBTS for devices with different PL configurations: 0 nm T-Al_2O_3 (a) without and (b) with intermediate O_2 plasma treatment, and with T-Al_2O_3 PL thicknesses of (c) 0.25, (d) 0.5, and (e) 0.75 nm

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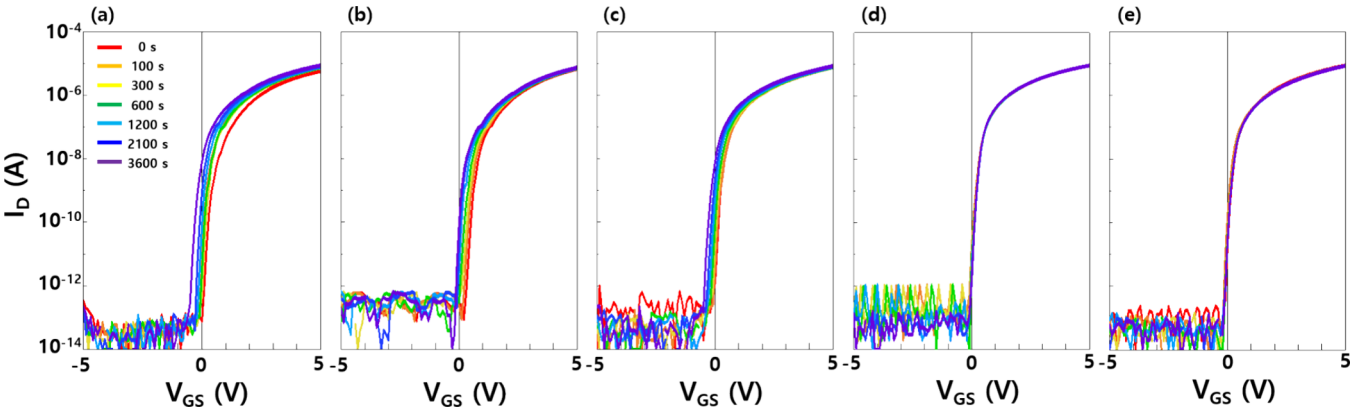


Figure 9. Evolution of the transfer characteristics of In_2O_3 TFTs during NBIS for devices with different PL configurations: 0 nm T-Al_2O_3 (a) without and (b) with intermediate O_2 plasma treatment, and with T-Al_2O_3 PL thicknesses of (c) 0.25, (d) 0.5, and (e) 0.75 nm.

drastic improvement in PBTS stability. Furthermore, elevating the stress temperature to 85 °C resulted in a mere V_{on} shift of 0.33 V (Figure S10). This enhancement is driven by the synergistic mechanisms provided by the T-Al_2O_3 layer. As it becomes thicker, it increasingly acts as a physical buffer, protecting the active channel from plasma-induced damage during the subsequent PEALD Al_2O_3 deposition and thereby suppressing new defect generation.[46] Simultaneously, consistent with the XPS and SIMS results, it acts as an active reservoir supplying hydrogen to passivate pre-existing oxygen-related defects at the interface. Although the individual contributions of physical plasma shielding and hydrogen-mediated defect passivation cannot be quantitatively decoupled, these mechanisms collectively play a crucial role in suppressing device instability under prolonged positive bias stress conditions.

To further evaluate the operational reliability of the fabricated TFTs, we investigated their stability under negative bias illumination stress (NBIS). The NBIS measurements were conducted for 3600 s by applying a constant gate electric field of −1 MV/cm under light irradiation at 1 mW/cm^2 using a halogen lamp.[26] In typical OSs, NBIS-induced degradation is widely attributed to the photo-induced ionization of neutral V_O defects.[15,69] Among the oxygen-related defect states reported in OSs, V_O are widely recognized as deep-level defects that can be photo-ionized under NBIS conditions ($V_O \rightarrow V_O^+ + e^-$, $V_O \rightarrow V_O^{2+} + 2e^-$).[15,69] The resulting positively charged donor-like states accumulate near the GI/OS interface and contribute to the negative shift in V_{on}. Due to the relatively low binding energy between indium and oxygen, In_2O_3 intrinsically contains a high density of these oxygen vacancies, which significantly deteriorate its NBIS stability. When comparing the two devices without a T-Al_2O_3 layer (Figure 9a,b), both exhibited substantial negative V_{on} shifts of −0.60 V and −0.55 V, respectively. However, the insertion of merely 0.25-nm of T-Al_2O_3 within the PL effectively suppressed the negative V_{on} shift to −0.40 V in Figure 9c. Furthermore, Figure 9d,e illustrate that increasing the T-Al_2O_3 thickness to 0.5-nm and 0.75-nm resulted in negligible V_{on} shifts. This profound improvement in NBIS stability is consistent with the hydrogen incorporation from the T-Al_2O_3 layer revealed by the SIMS analysis. The diffused hydrogen acts as a highly effective defect passivator by occupying the neutral V_O defects ($H_i^+ + V_O \rightarrow H_O^+$).[51,55] By converting these vulnerable defects into stable bonds, the hydrogen incorporation eliminates the primary source of photo-ionization. Ultimately, the device incorporating 0.75-nm of T-Al_2O_3 demonstrated the most optimized operational stability against photo-induced stress.

4. CONCLUSIONS

In conclusion, we successfully demonstrated a multifunctional PL architecture for top-gate PEALD In_2O_3 TFTs by introducing an *in situ*, plasma-free T-Al_2O_3 layer immediately following ultrathin channel deposition. Precise sub-nanometer control of the T-Al_2O_3 thickness enabled the layer to simultaneously function as a physical barrier against photolithography chemicals and subsequent O_2 plasma damage, while enabling controlled hydrogen incorporation into the In_2O_3 channel. Systematic analyses, including SIMS, depth-profile XPS, and high-frequency MIS $C-V$ measurements, indicated that controlled hydrogen incorporation modified the interfacial defect chemistry through the passivation of oxygen-related defects and suppression of interface trap density while concurrently contributing shallow donor states to optimize the carrier concentration. Consequently, the optimized top-gate TFT exhibited an exceptional field-effect mobility of 66.7 cm^2 V^{-1} s^{-1}, negligible hysteresis, and excellent switching characteristics. Concurrently, the T-Al_2O_3 layer significantly improved device reliability, which is attributed to its combined plasma-shielding and hydrogen-mediated defect-passivation effects. yielding a minimal PBTS-induced V_{on} shift of only 0.26 V and excellent resistance to NBIS degradation. Most importantly, these high-performance electrical characteristics and reliability enhancements were achieved through a completely thermal annealing-free process with a maximum process temperature of only 200 °C. The proposed multifunctional PL strategy provides a powerful platform for simultaneous physical separation from direct chemical exposure, mitigation of plasma-induced damage, and controlled hydrogen incorporation in oxide semiconductor devices, enabling significant improvements in both electrical performance and operational reliability.

■ ASSOCIATED CONTENT

Supporting Information

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Cross-sectional TEM image and corresponding EDS elemental mapping of the fabricated TGBC In_2O_3 TFT; $C-V$ curves of In_2O_3 TFT gate insulators with with varying T-Al_2O_3 thicknesses in the PL: 0 nm with O_2 plasma, 0.25 nm, 0.5 nm, and 0.75 nm.; output curves of TFTs with varying T-Al_2O_3 thicknesses in the PL: (a) 0 nm without O_2 plasma, (b) 0 nm with O_2 plasma, (c) 0.25 nm, (d) 0.5 nm, and (e) 0.75 nm.; contact resistance (RC) extracted using the *Y*-function method as a function of T-Al_2O_3 thickness within the PL.; transfer characteristics of In_2O_3 TFTs illustrating (a) a device with a 2-nm-thick T Al_2O_3 layer and (b) a device with a 0.75-nm-thick T-Al_2O_3 layer fabricated without intermediate O_2 plasma treatment.; XPS O 1s spectra of the 10-nm PEALD Al_2O_3 bulk layer: (a) without and (b) with the intermediate O_2 plasma treatment.; $C-V$ characteristics of a MIS capacitor fabricated without the T-Al_2O_3 layer (0 nm) and intermediate O_2 plasma treatment.; First-derivative (dC/dV) plots of the $C-V$ characteristics for devices with T-Al_2O_3 thicknesses of (a) 0, (b) 0.25, (c) 0.5, and (d) 0.75 nm within the PL under forward and reverse voltage sweeps. The extracted ΔV_{FB} values are approximately 0.9, 0.5, 0.3, and 0.1 V, respectively.; First-derivative (dC/dV) plots of the $C-V$ characteristics for the 0-nm T-Al_2O_3 devices (a) without and (b) with O_2 plasma treatment of the bulk PL.; Transfer characteristic shifts under PBTS at an elevated temperature of 85 °C (1 MV/cm, 3600 s) for the optimized TFT with a 0.75-nm T-Al_2O_3 layer (DOCX)

AUTHOR INFORMATION

Corresponding Author

Sang-Hee Ko Park − *Department of Materials Science and Engineering, Korea Advanced Institute of Science and Technology (KAIST), 291 Daehak-ro, Yuseong-gu, Daejeon 305-701, Republic of Korea;* orcid.org/0000-0001-7165-8211; Email: shkp@kaist.ac.kr

Authors

Sunghwan Park − *Department of Materials Science and Engineering, Korea Advanced Institute of Science and Technology (KAIST), 291 Daehak-ro, Yuseong-gu, Daejeon 305-701, Republic of Korea;* orcid.org/0009-0007-5361-6684

Hwa Young Kim − *Department of Materials Science and Engineering, Korea Advanced Institute of Science and Technology (KAIST), 291 Daehak-ro, Yuseong-gu, Daejeon 305-701, Republic of Korea*

Tae Hwan Boo − *Department of Materials Science and Engineering, Korea Advanced Institute of Science and Technology (KAIST), 291 Daehak-ro, Yuseong-gu, Daejeon 305-701, Republic of Korea*

Hunbeom Shin − *Department of Materials Science and Engineering, Korea Advanced Institute of Science and Technology (KAIST), 291 Daehak-ro, Yuseong-gu, Daejeon 305-701, Republic of Korea*

Seonghyun Kim − *Department of Materials Science and Engineering, Korea Advanced Institute of Science and Technology (KAIST), 291 Daehak-ro, Yuseong-gu, Daejeon 305-701, Republic of Korea;* orcid.org/0009-0001-1853-7733

Seungbum Hong − *Department of Materials Science and Engineering, Korea Advanced Institute of Science and Technology (KAIST), 291 Daehak-ro, Yuseong-gu, Daejeon 305-701, Republic of Korea;* orcid.org/0000-0002-2667-1983

Complete contact information is available at: https://pubs.acs.org/doi/10.1021/acsaelm.6c01911

Author Contributions

S.H.P.: conceptualization, investigation, methodology, formal analysis, visualization, validation, and writing original draft. H.Y.K.: methodology and investigation. T.H.B.: methodology and investigation. H.B. Shin: methodology and investigation. S.H.K. and S.H.: AFM analysis. S.-H.K.P.: supervision and review & editing.

Notes

The authors declare no competing financial interest.

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