Memristive Logic-in-Memory Integrated Circuits for Energy-Efficient Flexible Electronics

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A memristive nonvolatile logic-in-memory circuit can provide a novel energy-efficient computing architecture for battery-powered flexible electronics. However, the cell-to-cell interference existing in the memristor crossbar array impedes both the reading process and parallel computing. Here, it is demonstrated that integration of an amorphous In-Zn-Sn-O (a-IZTO) semiconductor-based selector (1S) device and a poly(1,3,5-trivinyl-1,3,5-trimethyl cyclotrisiloxane) (pV3D3)-based memristor (1M) on a flexible substrate can overcome these problems. The developed a-IZTO-based selector device, having a Pd/a-IZTO/Pd structure, exhibits nonlinear current–voltage (*I–V*) characteristics with outstanding stability against electrical and mechanical stresses. Its underlying conduction mechanism is systematically determined via the temperature-dependent *I–V* characteristics. The flexible one-selector–one-memristor (1S–1M) array exhibits reliable electrical characteristics and significant leakage current suppression. Furthermore, single-instruction multiple-data (SIMD), the foundation of parallel computing, is successfully implemented by performing NOT and NOR gates over multiple rows within the 1S–1M array. The results presented here will pave the way for development of a flexible nonvolatile logic-in-memory circuit for energy-efficient flexible electronics.

1. Introduction

Portable electronics, such as smart phones and tablets, are at the core of the electronics industry, which is creating worldwide economic growth. However, recent rapid technological advances have generated a slowdown in the economic growth by portable electronics; thus, new breakthroughs are required to stimulate the electronics market. To revitalize this market, flexible and wearable electronics have been investigated as next-generation electronics; these devices would offer outstanding convenience, portability, and human-friendly interfaces.[1] Flexible logic and memory devices, in particular, are regarded as essential components of electronic systems because of their roles in information processing, storage, and communication with external devices. Several research groups have developed a variety of organic thin-film transistor (OTFT)-based flexible logic gates and memories. Although these OTFT-based devices have been fabricated in a cost-effective manner with superior flexibility over a large area on flexible substrate, there remain inherent problems related to device performance and power consumption. One of the most significant difficulties is the high static power consumption of these devices, as flexible and wearable electronics have a limited battery supply and a long standby period. This problem arises because of the volatile computing architecture in current processors, which is composed of a volatile working memory and volatile transistor-based logic circuit.[2,3] In addition, the use of von Neumann architecture, with its physically separate memory and processor, generates an extremely large energy-hungry data transfer between the memory and processor, inducing long latency and high power consumption.[4]

The memristor has been proposed as the fourth fundamental circuit element[5,6] and can provide a creative solution to these problems. The memristor device has been widely investigated for a promising nonvolatile memory due to its simple structure, fast switching speed, low power consumption, and high packing density.[7,8] Furthermore, memristors can implement a nonvolatile logic-in-memory circuit, enabling construction of a novel nonvolatile computing architecture. In such a circuit, the memristor device can act as both a nonvolatile memory and a logic gate in the memristor crossbar array, enabling not only a novel energy-efficient computing architecture via data-transfer elimination, but also normally off computing with a static power consumption of 0 W.[9–12]

The crossbar array is the optimal architecture enabling high packing density, defect tolerance, and logic operation;[13,14] however, this architecture generates an inherent cell-to-cell

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DOI: 10.1002/adfm.201704725

interference problem.[15] As this interference allows undesirable leakage currents known as "sneak currents" to flow through unselected devices during memristor operations, it limits the maximum array size and prevents the memristive nonvolatile logic-in-memory circuit from enabling parallel computing.[16] These sneaky currents have limited experimental demonstrations to logic operations in only a row of devices,[12,17] along with a number of iterative sequential steps for logic operation across many rows in a memristor crossbar array (which implies the worst latency).[18] Therefore, in order to mitigate these problems, a memristor device should be integrated with two-terminal selector device to obtain a highly integrated one-selector–one-memristor (1S–1M) array. The selector device should have a symmetric current–voltage (I–V) nonlinearity, which blocks the current flow at a low-voltage region while allowing a significantly larger (e.g., >100×) current in a higher-voltage region.[19]

Many research groups have explored various two-terminal selector devices, such as the back-to-back Schottky diode,[20] threshold switching device,[21] mixed-ionic conductor device,[22] and multilayer tunneling device.[19,23] In particular, the back-to-back Schottky diode is preferred as a flexible selector device because of its easy fabrication on plastic substrate, low-temperature process, and simple design. However, only a small number of reports on flexible selector devices have been published to date that have focused on the back-to-back Schottky diode with Ni/TiO_2/Ni structure for only nonvolatile flexible memory application.[24,25] Certain problems are associated with this TiO_2-based flexible selector device, such as the requirement for well-controlled stoichiometry and crystallinity of the TiO_2 and insufficient current density due to the low carrier mobility of this material. Therefore, development of a new amorphous semiconductor material with high carrier mobility, easy stoichiometry controllability, and excellent flexibility for practical flexible memristive logic-in-memory circuit application is important.

Amorphous-oxide-semiconductor (AOS) thin films have received considerable attention as active layers in flexible thin-film transistors (TFTs) because of their inherent amorphous properties that enable high device-to-device uniformity, low manufacturing cost, and high transparency.[26,27] Among the various types of AOS, amorphous In-Zn-Sn-O (a-IZTO) is a promising material for TFT because of its high electron mobility (20–30 $cm^2\ V^{-1}\ s^{-1}$), low process temperature, and low off-current due to a wide band gap.[28] In addition to TFT application, a-IZTO is desirable as an active material for flexible selector device development based on the back-to-back Schottky diode. However, it is generally challenging to form a stable Schottky contact between a metal and oxide semiconductor (OS) because of the surface electron accumulation layer (SEAL) that naturally arises from OS surfaces reduced in a vacuum chamber.[29–32] Thus, several methods of solving this problem have been proposed, such as deposition of a conducting polymer on the OS to hinder SEAL formation[33] and SEAL removal using a chemical surface treatment[34,35] or oxygen plasma treatment.[31,32,36,37] Among these solutions, oxygen plasma treatment on the OS surface is suitable for the development of a flexible back-to-back Schottky diode-type selector device because the plasma treatment process can provide a uniform and reliable selector device on the plastic substrate with high oxidation speed at low temperature. Although a-IZTO with high electron mobility is available, along with a strong oxygen plasma-treated Schottky contact on a plastic substrate, no attempts have been made to apply this technology to a memristive logic-in-memory circuit as well as selector device development, even on a rigid substrate.

Herein, we develop a 1S–1M integrated circuit using a poly (1,3,5-trivinyl-1,3,5-trimethyl cyclotrisiloxane) (pV3D3)-based memristor and an a-IZTO-based selector on a flexible polyethersulfone (PES) substrate to propose a conceptual strategy for realizing an energy-efficient memristive nonvolatile logic-in-memory circuit, enabling parallel computing. The fabricated flexible a-IZTO-selector device exhibits outstanding stability against harsh electrical stress and mechanical strain. Using X-ray photoelectron spectroscopy (XPS) analysis and examining the I–V characteristics, effective removal of the a-IZTO SEAL via oxygen plasma treatment is confirmed. Thanks to this reliable and flexible a-IZTO selector, the 1S–1M integrated devices exhibit a significantly reduced leakage current under a low-voltage region compared to a 1M device, along with reliable switching performance against electrical and mechanical stresses. The reading margin of the 1S–1M array is evaluated under various operational schemes (ground, V/2, V/3), indicating a feasible maximum array size of more than 1 Mbit. We also experimentally demonstrate that the fabricated 1S–1M array can perform single-instruction multiple-data (SIMD), the basis of parallel computing, without interruption by the sneak current. We strongly believe that the proposed parallel computing method using a memristive nonvolatile logic-in-memory circuit can provide a low-power circuit platform for battery-powered flexible electronic systems with various potential applications.

2. Results and Discussion

2.1. Flexible 1S–1M Cell Array

Figure 1a schematically illustrates the operation process in a memristor crossbar array on a flexible substrate. During this process, if there is no selector device, the sneak currents flow through the unselected cells, as indicated by the red dotted lines in Figure 1a, resulting in a readout process error. Furthermore, the SIMD, on the basis of parallel computing,[38] which performs the same operation on multiple data in parallel, is prevented by the sneak current in the memristive nonvolatile logic-in-memory circuit (see Figure S1 in the Supporting Information for details of sneak current affecting parallel computing). To overcome this problem, we developed a flexible selector device with a Pd/a-IZTO/Pd structure on a flexible PES substrate, the working principle of which is based on the back-to-back Schottky diode. Figure 1b shows the I–V characteristics of a-IZTO-selector devices, with and without oxygen plasma treatment of the a-IZTO surface prior to top Pd electrode deposition. Note that the presence of a SEAL in the a-IZTO is clearly indicated by the almost ohmic behaviors exhibited by the a-IZTO-selector devices that were not subjected to oxygen plasma treatment. In contrast, the oxygen plasma-treated devices exhibit nonlinear I–V characteristics, which suppress

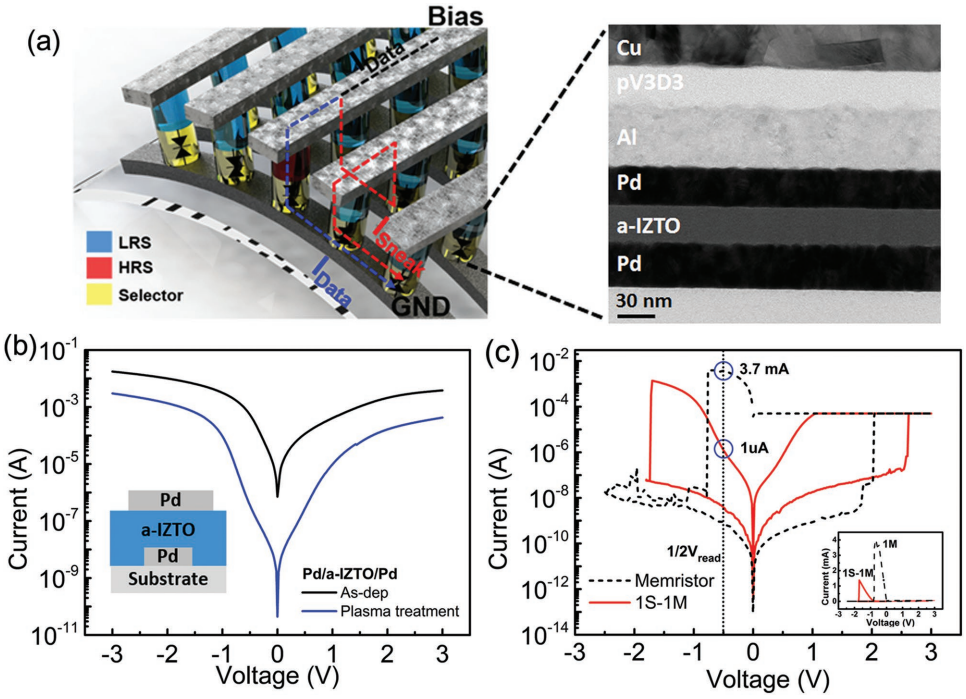

Figure 1. a) Schematic illustration of integrated selector device role in memristor crossbar array during operation, and cross-sectional TEM image of 1S–1M device. b) *I–V* characteristics of a-IZTO-selector devices without and with oxygen plasma treatment. c) Comparison of *I–V* characteristics of 1S–1M and 1M devices. Inset: Nonlinear *I–V* characteristics of 1S–1M device on linear scale compared with 1M device.

the current flow in either direction in the low-voltage region, while allowing a significantly larger current in the high-voltage region. These *I–V* characteristics imply that oxygen plasma treatment is an effective strategy toward Schottky barrier formation by removing the SEAL from a-IZTO on a plastic substrate.

To confirm the feasibility of the a-IZTO-selector device for application as a selector device in memristor crossbar array, we vertically integrated the flexible a-IZTO-selector device with the flexible memristor device. For the latter, a pV3D3-memristor device with Cu/pV3D3/Al structure was selected for integration with the flexible a-IZTO-selector device because of its reliable switching characteristics without a passivation layer, outstanding mechanical stability, and good uniformity on a flexible substrate (via solvent-free initiated chemical vapor deposition (iCVD)) compared to other polymer-based flexible memristors.[39] The pV3D3-memristor operates with a Cu filament, whose formation via electrochemical reaction and rupture via Joule heating inside the pV3D3 induces low resistance states (LRS) and high resistance states (HRS), corresponding to logical "1" and "0", respectively. The inset of Figure 1a exhibits a cross-sectional high-resolution transmission electron microscopy (HRTEM) image of the fabricated 1S–1M integrated device (see Figure S2 in the Supporting Information for optical microscope image of the fabricated 1S–1M integrated device). Hence, it is confirmed that the thin (≈30 nm) a-IZTO film was formed uniformly between the top and bottom Pd electrodes in the lower layer of HRTEM image. As shown in the upper layer of HRTEM image, the pV3D3-memristor, which consists of top Cu electrode, pV3D3 films, and bottom Al electrode, was successfully formed on a-IZTO selector device. Further, the chemical composition of the 1S–1M integrated device was verified through transmission electron microscopy (TEM) energy dispersive X-ray spectroscopy (EDX) elemental mapping (Figure S3, Supporting Information). The results indicate that the thin film between the Pd electrodes was composed of In (green), Zn (blue), Sn (bluish green), and O (purple).

The *I–V* characteristics of the integrated flexible 1S–1M memristor with a-IZTO-selector and pV3D3-memristor are presented in Figure 1c. By integrating the pV3D3-memristor onto the a-IZTO-selector, the leakage current of the 1S–1M at $V_{READ}/2$ was reduced significantly, by more than three orders of magnitude compared to the linear *I–V* characteristics of the 1M device. As shown in the inset of Figure 1c, the reduced currents in the low-voltage region clearly originate from the nonlinear *I–V* characteristics of the a-IZTO-selector device. Therefore, this result indicates that the flexible a-IZTO-selector device is suitable for effective suppression of the sneak currents in the memristor crossbar array on the flexible substrate.

2.2. Electrical Characterization of Flexible a-IZTO-Selector

To investigate the electrical stability of the fabricated flexible a-IZTO-selector device, constant bias stability and cycling endurance tests were conducted. **Figure 2**a shows the results of a constant bias stability test conducted under a constant voltage stress of −3 V for 10^4 s to confirm the stability of the top Schottky barrier formed via the oxygen plasma treatment. The *I–V* curves of the selector device shifted toward the negative voltage region by 110 mV under the bias stress, originating from electron trapping at the top Pd/a-IZTO interface. The results of the cycling endurance test conducted under repeated

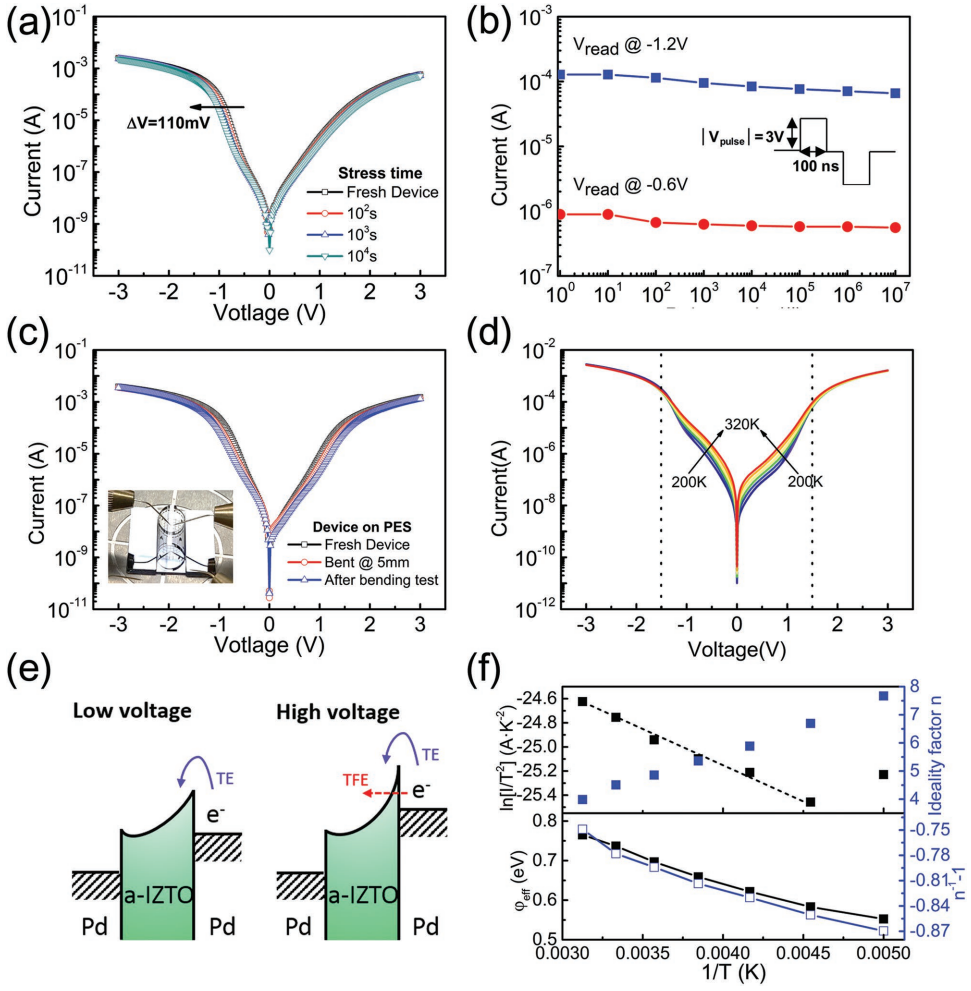

Figure 2. a) *I–V* characteristics of a-IZTO-selector device under constant bias stress. b) Cycling endurance performance of a-IZTO-selector device. c) *I–V* characteristics of a-IZTO-selector device before bending test, when bent, and after bending. Inset: Photograph of *I–V* measurement being performed under bent conditions. d) Temperature-dependent *I–V* characteristics of a-IZTO-selector device. e) Schematic of a-IZTO-selector device conduction mechanisms under low- and high-voltage regions. f) Richardson plot and temperature dependence of n, φ_{eff}, and (n^{-1}–1) under negative voltage region.

voltage pulses are shown in Figure 2b. In this test, voltage pulses with 100 ns width and ±3 V amplitude were applied over 10^7 cycles. Following the pulse application, the read currents at the read voltages V_{READ} (−1.2 V) and $V_{READ}/2$ (−0.6 V) were measured according to the V/2 reading scheme.[40] As shown in Figure 2a, the currents at V_{READ} and $V_{READ}/2$ decreased gradually during the cycling endurance test, as a result of electron trapping in the Pd/a-IZTO interface. However, the nonlinearity between currents at V_{READ} and $V_{READ}/2$ was sustained without significant degradation; thus, the cycling endurance test did not deteriorate the flexible a-IZTO-selector device. Furthermore, to confirm its feasibility for flexible device application, the a-IZTO-selector device on plastic substrate was evaluated via a bending test. As shown in Figure 2c, a fresh device (black), the device subjected to a 5 mm bending radius (red), and the post-bending-test device (blue) exhibited similar *I–V* characteristics with no noticeable degradation, indicating the excellent mechanical robustness of the flexible a-IZTO-selector device. As the electrical and mechanical stability of the selector device is an essential requirement for flexible memristive logic-in-memory circuit applications, these results indicate that the flexible a-IZTO-selector device can constitute a high-density memristor array on a flexible substrate.

In order to analyze the conduction mechanism of the a-IZTO-selector, we investigated the temperature dependence of the *I–V* characteristics of the a-IZTO-selector device, as shown in Figure 2d. Note that two distinct regions exist according to the temperature-dependent *I–V* behavior. In the high-voltage region ($|V| > 1.5$ V), the measured current exhibits little temperature dependence, indicating that the tunneling conduction is the dominant conduction mechanism. On the other hand, in the low-voltage region ($|V| < 1.5$ V), strong temperature dependence can be observed for the measured current, implying thermionic emission over the Pd/a-IZTO barrier. Hence, we can infer that the conduction mechanism is based on thermionic emission ($|V| < 1.5$ V) and thermionic field emission ($|V| > 1.5$ V) across the Schottky barrrier (Figure 2e). The linearity in the Richardson plots extracted from

the low negative and low positive voltage regions (Figure 2f and Figure S4, Supporting Information, respectively) also indicates that the dominant conduction mechanism in the low-voltage region is governed by thermionic emission. However, large deviations from the straight line are apparent at 200 K.[41] This behavior indicates that the thermionic emission observed in the low-voltage region can be explained by not a simple uniform Schottky junction model but a barrier height fluctuation model.[42] In the barrier height fluctuation model, the barrier height has a Gaussian distribution with $\varphi_{eff} = \varphi_m - q\sigma^2/(2k_BT)$, where φ_{eff} is the effective barrier height, φ_m is the mean barrier height, and σ is the standard deviation of barrier height. Furthermore, φ_{eff} and $(n^{-1} - 1)$ exhibit relatively linear behavior as functions of T^{-1}, implying an inhomogeneous barrier height.[41] As in the case of the Schottky contact of an AOS,[43] this barrier height inhomogeneity may originate from the a-IZTO grain boundaries, oxygen deficiency, and the different crystallographic surfaces of the Pd. A clear analysis of the conduction mechanism of the a-IZTO-selector device can present guidelines for structural design and comprehensive modeling of selector devices.

2.3. Analysis of O_2 Plasma Treatment Effect through XPS

For detailed investigation of the effect of the oxygen plasma treatment on the a-IZTO film, a composition analysis of the a-IZTO was conducted via XPS. To calibrate the spectra, the C 1s level (285.0 eV) was used.[44] **Figure 3**a,b shows representative XPS spectra of the O 1s core levels for a-IZTO film without and with oxygen plasma treatment, respectively. A clear difference is apparent between the two O 1s spectra; that is, increased

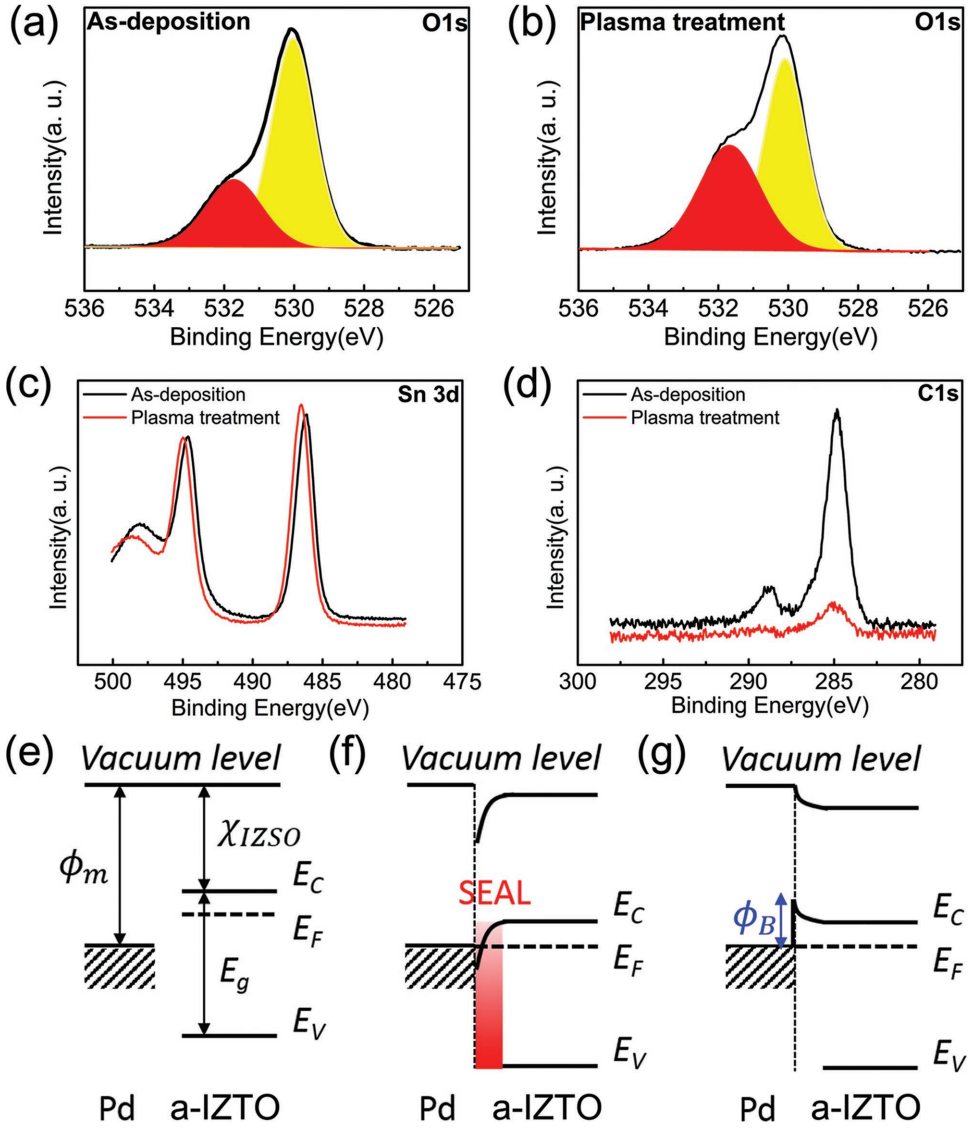

Figure 3. O1s core level spectra of a) as-deposited and b) oxygen plasma-treated a-IZTO thin film. c) Sn 3d and d) C 1s core level spectra of a-IZTO thin films without and with oxygen plasma treatment. Schematic band diagram for e) Pd and a-IZTO prior to contact, f) Pd contact on as-deposited a-IZTO with SEAL, and g) Pd contact on oxygen plasma-treated a-IZTO with Schottky barrier at interface.

peak intensity is obtained with a higher binding energy after the oxygen plasma treatment. Each O 1s core level consists of two peaks: 530 and 531.9 eV. The O 1s peak with the lower binding energy corresponds to M—O bonds (M = In, Zn, and Sn), whereas the higher binding energy corresponds to O—H, O—C, and O—O bonding adsorbed on the a-IZTO surface.[45–47] Here, the effect of the contaminated hydrogen and carbon species on the a-IZTO surface is neglected, because these species easily react with oxygen radicals and are, therefore, eliminated during oxygen plasma treatment.[48] Accordingly, the increased intensity for higher binding energy is primarily regarded as being due to O—O bonding (O^- ions) adsorbed on the a-IZTO surface. As previously reported, the adsorbed oxygen on the oxide surface due to the oxygen plasma can eliminate the accumulation layer and generate a surface depletion region.[37,47] Furthermore, we also found that the peak binding energies of the other core levels, such as Sn 3d, In 3d, and Zn 2p, shift toward higher values, as shown in Figure 3c (see Figure S5 in the Supporting Information for the In 3d and Zn 2p levels). Given that the positions of the two C 1s peaks with and without oxygen plasma treatment exhibit close correspondence (Figure 3d), the higher binging energy shifts of the other core levels indicate that the a-IZTO surface was oxidized by the oxygen plasma treatment. Therefore, based on the XPS analysis, it can be concluded that the oxygen plasma treatment method can sufficiently eliminate the SEAL in a-IZTO, resulting in the formation of a Schottky barrier between the Pd and a-IZTO.

Figure 3e–g are schematic illustrations of the band structure constructed based on the above results. Figure 3e shows the energy band diagram for Pd and n-type a-IZTO before contact formation. In general, at the interface between a semiconductor and metal, the Schottky barrier height ϕ_B is given by $\phi_B = \phi_M - \chi$, where ϕ_M is the metal work function and χ is the electron affinity of the semiconductor. Here, the band gap (3.08 eV) and χ (4.5 eV) of a-IZTO were extracted from the ultraviolet photoemission spectroscopy (UPS) and UV–vis spectroscopy results (Figure S6, Supporting Information). The ϕ_{Pd} value (5.22 eV) was adopted from the literature.[49] Note that the theoretical ϕ_B between Pd and a-IZTO is expected to be larger than 0.72 eV. However, the naturally formed SEAL of the as-deposited a-IZTO film hinders the formation of a Schottky barrier, as indicated by the almost ohmic behavior of the *I–V* characteristics (Figure 1b). Thus, the energy band diagram for the Pd contact on the as-deposited a-IZTO film exhibits surface band bending, as shown in Figure 3f. In contrast, the oxygen-plasma-treated a-IZTO-selector devices exhibit nonlinear *I–V* characteristics, indicating the existence of a Schottky barrier at the Pd/a-IZTO interface. Finally, the energy band diagram of the Pd contact on the oxygen plasma-treated a-IZTO film was determined based on the nonlinear *I–V* characteristics and XPS results, as shown in Figure 3g.

2.4. Reading Margin and Electrical Characterization of 1S–1M Array

For the reading operation of the memristor device in the crossbar array, three reading bias schemes were proposed: ground, V/2, and V/3, as shown in **Figure 4**a. In the ground scheme, all the unselected word and bit lines were grounded. As a result, the V_{READ} were only applied to the cells with a selected word line, where most sneak currents occur. In the V/2 scheme, all the unselected word and bit lines were biased at half the read voltage ($V_{READ}/2$), allowing the sneak currents to flow through the half-selected cells in the selected word and bit lines. In the V/3 scheme, all the unselected word and bit lines were biased at one-third ($V_{READ}/3$) and two-thirds ($2V_{READ}/3$) of the read voltage, respectively, thereby triggering sneak currents through all the one-third selected cells, except for the selected cells in the crossbar array.

To evaluate the realizable maximum array size of the flexible 1S–1M, the reading margin in the crossbar array was calculated. In the numerical calculation, the worst case scenario (all unselected cells with LRS) was considered, and the three reading bias schemes (ground, V/2, and V/3) were evaluated to determine the optimal reading bias scheme. The numerical solution of the reading margin calculation was obtained using MATLAB (Figure S7, Supporting Information). A 10% reading margin was set as the criterion for determining the maximum crossbar array size. It was found that the ground scheme exhibits the highest reading margin (Figure 4b). On the other hand, the V/2 and V/3 schemes exhibit significant reading margin degradation with increasing array size. The obvious differences in reading margin among the three reading schemes arises from the source of the sneak currents; the ground scheme generates leakage current from the cells with the selected word line only, whereas the other two schemes induce leakage currents from all half and one-third selected cells on the crossbar array. However, the ground scheme dissipates more power than the V/2 and V/3 schemes;[40] thus, the V/2 and V/3 schemes are more desirable for realization of a battery-powered flexible electronic system. Note that the use of two V/2 and V/3 schemes enables the 1S–1M array size to be increased to 1 Mbit, indicating the feasibility of the high-density flexible memristive nonvolatile logic-in-memory circuit.

To investigate the reliability of the flexible 1S–1M memristor, cycling endurance and retention tests were conducted. As shown in Figure 4c, stable operation without noticeable degradation was observed for the 1S–1M device under severe electrical stresses and for more than 10^4 cycles. Furthermore, after the cycling endurance tests, the retention characteristics of the flexible 1S–1M device were evaluated at V_{READ} (–1 V) and $V_{READ}/2$ (–0.5 V). Stable retention was confirmed for 10^5 s without noticeable degradation of the nonlinearity (Figure 4d). The operational device yield of the flexible 1S–1M memristor is ≈80% without an additional optimization of the fabrication process (20 successes out of 25 cells), and the device-to-device distribution of resistance states at V_{READ} and $V_{READ}/2$ extracted from 20 unit cells exhibits a narrow distribution without overlap (Figure S8, Supporting Information). In addition, the flexible 1S–1M memristor exhibited good mechanical stability without significant degradation during repeated bending over 1000 cycles at a bending radius of 5 mm (Figure 4e). These outstanding electrical and mechanical stabilities are attributed to the electrically and mechanically robust a-IZTO-selector and pV3D3-memristor. Although the endurance of the flexible 1S–1M device can be acceptable for some memory application, this endurance may be poor for general purpose logic

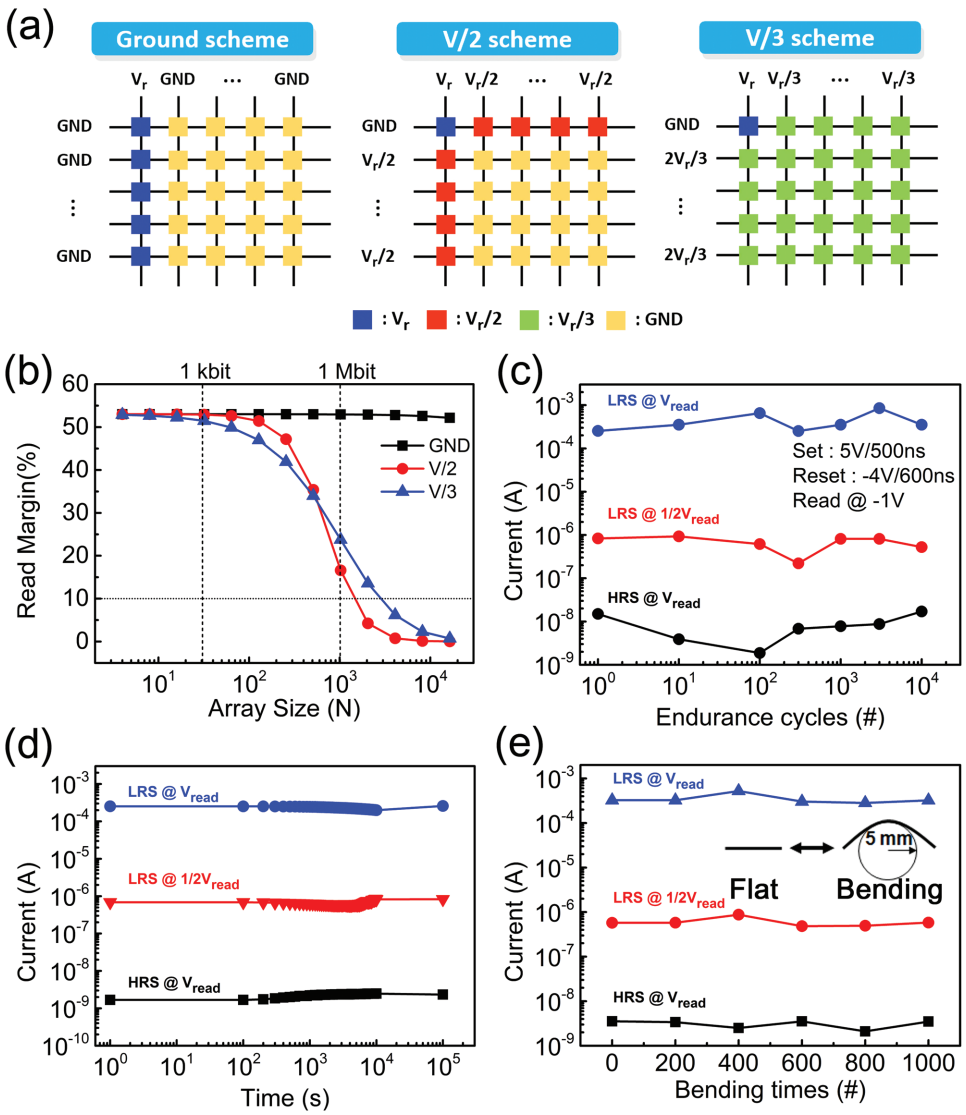

Figure 4. a) Three reading bias schemes in memristor crossbar array: ground, V/2, and V/3 schemes. b) Calculated reading margin comparison for three reading bias schemes as function of array size. c) Cycling endurance performance, and d) retention characteristics of 1S–1M device. e) Repetitive bending fatigue test for 1S–1M device.

operations. However, we believe that the intensive improvement would be achieved by adopting a chemical mechanical polishing process to flatten electrodes because rough surface of electrodes naturally arose from multistacking results in the weak points where the localized electric field is enhanced.[50]

2.5. Parallel Computing of Logic-in-Memory Circuit within 1S–1M Array

Parallel computing of the memristive nonvolatile logic-in-memory circuit within the 1S–1M array was achieved using memristor-aided logic (MAGIC) architecture. This architecture requires only a voltage pulse and memristors within a crossbar array to implement the logic gate,[51] as shown in **Figure 5**. The simple MAGIC architecture allows for more reliable implementation of the memristive logic circuit on the flexible substrate compared to the memristor-materials implication (IMP) logic architecture.[11] In addition, the MAGIC architecture has advantages in terms of latency (2.4 times) and power consumption (less than 33.7%) compared to those of the IMP.[16] Logic gates using MAGIC architecture were realized within the crossbar array via two steps: initialization of the output memristor to logical "1" and the conditional logic operation of the output memristor achieved by applying a pulse voltage V_0 across the memristors for a specific input memristor combination. The NOT and NOR gates, which are well-known universal logic gates, can be implemented using the MAGIC architecture, enabling implementation of additional logic gates via an appropriate network. For reliable logic operation, the voltage drop across the initialized output memristor during application of V_0 should be sufficiently high to switch its logical state. Therefore, for measurement convenience, we chose a V_0 of −4 V with a 5 ms pulse width.

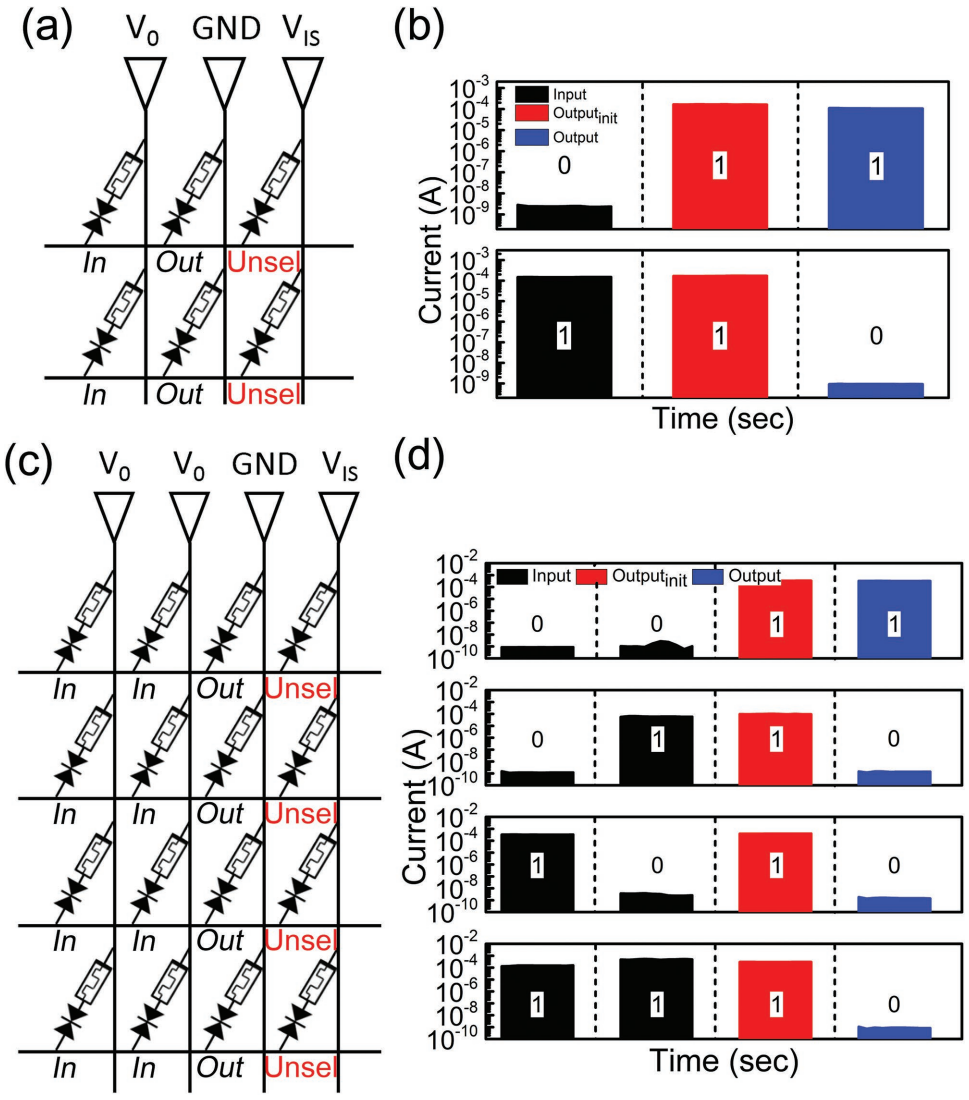

Figure 5. Parallel logic operations within 1S–1M memristor array. a) Schematic of MAGIC-NOT gates within 1S–1M memristor array. b) Experimental results for parallel operation of MAGIC-NOT gates. c) Schematic of MAGIC-NOR gates within 1S–1M memristor array. d) Experimental results for parallel operation of MAGIC-NOR gates.

To confirm the adverse effect of the sneak current on the logic operation, we analyzed the current flowing through the unselected cells in the crossbar array via PSPICE, which is a general-purpose circuit simulator. During the parallel logic operation, we considered the worst case scenario, in which all devices that do not participate in the logic operation are programmed to logical "1." It was observed that the initialized output memristor with logical "1" could be destroyed by the high sneak current through the unselected cells (Figure S9a, Supporting Information). Thus, to overcome this problem, the memristors were integrated with selectors and an isolation voltage V_{IS} of –0.5 V was applied to the unselected columns. As shown in Figure S9b in the Supporting Information, by integrating the selectors and applying V_{IS}, the current flowing through the unselected cells can be exponentially suppressed as a result of the nonlinear selector I–V characteristics, enabling reliable parallel logic operation of the flexible memristive nonvolatile logic-in-memory circuit.

Based on the above simulation results, we experimentally demonstrated that the fabricated 1S–1M array can perform parallel logic operations. Figure 5a is a schematic of the MAGIC-NOT gates within the crossbar array. For parallel NOT logic operation, the memristor initialization was performed first (the input values for the input memristors and logical "1" for the output memristors are listed in the first and second columns, respectively). To implement the parallel logic operation under the worst case conditions, all unselected cells in the third column were programmed to LRS. The MAGIC-NOT operation was performed by applying V_0 and V_{IS} to the first and third columns, respectively, with the second column grounded. In the first row with the input memristor logical "0," V_0 primarily dropped across the input memristor via the voltage divider, maintaining the logical "1" of the initialized output memristor. In the second row with the input memristor logical "1," the applied voltage across the output memristor was higher than its reset voltage, which changed its state to logical "0." Thus,

NOT gates were implemented simultaneously in all rows. The measurement results shown in Figure 5b present reliable parallel operation of the MAGIC-NOT gates within the memristor crossbar array. Although the current of pV3D3-memristor logical "1" (≈100 μA) can cause significant dynamic power consumption of the memristive nonvolatile logic-in-memory circuit, the higher current of memristor logical "1" can reduce the latency by lowering resistive-capacitive (RC) delay.[16] Furthermore, it is noted that the memristive nonvolatile logic-in-memory circuit can realize both the low power consumption and a short interconnection delay compared with the conventional complementary logic circuit with the global interconnection because of its computing architecture with data-transfer elimination.[4] Therefore, any memristive logic-in-memory circuits can be optimized for the power consumption and latency constraints of the application.

In the same manner as the MAGIC-NOT gate, multiple MAGIC-NOR gates can be implemented simultaneously, as shown in Figure 5c. In the first row, where both input memristors are logical "0," the voltage drop across the output memristor is lower than its reset voltage, inducing retention of the initialized output memristor logical "1." On the other hand, for all the various rows with input memristor combinations (input 1, input 2: 01, 10, 11), the voltage applied across the output memristor is higher than its reset voltage, causing a switching of its state to logical "0." MAGIC-NOR gates were simultaneously achieved within the crossbar array, as shown in the measurement results presented in Figure 5d. However, these parallel MAGIC executions can cause the undesirable logic operation for unselected rows within memristor crossbar array. This problem is resolved by applying V_{IS} at the unselected rows (Figure S10, Supporting Information). This parallel computing of memristive nonvolatile logic-in-memory circuit is to perform simultaneously the logic operation over multiple rows, performing the SIMD architecture. The SIMD is a type of parallel computing architecture in Flynn's taxonomy,[38,52] enabling the single instruction to perform the same processing on multiple data in parallel. Considering that a modern computer is often a multiprocessor multiple-instruction multiple-data (MIMD) machine where each processor implements SIMD,[53] the parallel logic operation of memristive nonvolatile logic-in-memory circuit is powerful and energy-efficient. Therefore, we experimentally demonstrated that the parallel logic operations of the MAGIC-NOT and -NOR gates can be achieved through integration of the a-IZTO-selector and pV3D3-memristor. This result clearly shows the feasibility of the energy-efficient novel advanced computing architecture for the construction of practical flexible electronic systems.

3. Conclusion

In summary, we demonstrated that a memristive nonvolatile logic-in-memory integrated circuit using 1S–1M memristor arrays enables parallel computing. With AOS thin film, the a-IZTO-selector device exhibits nonlinear *I–V* characteristics, excellent cycling endurance, constant bias stability, and excellent mechanical stability. The temperature-dependent *I–V* behavior reveals that the dominant conduction mechanisms are thermionic emission and thermionic field emission for the low- and high-voltage regions, respectively. To demonstrate practical flexible selector device application, integrated 1S–1M memristor arrays with a-IZTO-selectors and pV3D3-memristors were fabricated and characterized. The 1S–1M device exhibited a leakage current reduced by more than three orders of magnitude in LRS, stable retention (>10^5 s), and excellent cycling endurance (10^4 cycles). The 1S–1M reading margin was also evaluated under different reading schemes, showing that the 1S–1M device can be feasibly applied in a memristor crossbar array with a high density of up to 1 Mbit. Furthermore, we experimentally demonstrated that the parallel logic operation of the NOT and NOR gates can be implemented using the 1S–1M cell array. Our research on integrated 1S–1M memristor arrays will reveal new possibilities toward the realization of flexible memristive logic-in-memory circuits, enabling parallel computing for an energy-efficient flexible electronic system.

4. Experimental Section

Pd/a-IZTO/Pd devices were fabricated with crossbar structures. First, 60 nm thick Pd electrodes were deposited on a PES substrate via thermal evaporation through a metal shadow mask. Then, a 30 nm thick a-IZTO film was deposited on the bottom Pd electrodes using radio frequency sputtering under high vacuum conditions (0.088 Pa) at room temperature. Before the top Pd electrode deposition, oxygen plasma treatment was performed to eliminate the SEAL in the a-IZTO using an inductively coupled plasma asher system (power = 100 W, O_2 flow = 50 sccm, pressure = 200 mTorr, time = 600 s). Finally, the device fabrication was completed by depositing 60 nm thick Pd electrode lines perpendicular to the bottom electrodes via thermal evaporation through the metal shadow mask.

To fabricate the 1S–1M array, a pV3D3-memristor with Cu/pV3D3/Al structure was fabricated on a-IZTO-selector device. 70 nm thick Al electrodes were patterned on a Pd/a-IZTO/Pd device via thermal evaporation through a metal shadow mask. Next, a 20 nm thick pV3D3 film was deposited on the Al electrodes via the iCVD process.[54] The 1S–1M device with Cu/pV3D3/Al/Pd/a-IZTO/Pd structure was completed by depositing a 60 nm thick Cu electrode via thermal evaporation through a metal shadow mask. All Line widths of Pd, Cu, and bottom Al electrodes were identical at 60 μm (see Figure S11 in the Supporting Information for details of the fabrication of the 1S–1M array).

To investigate the electrical characteristics of the fabricated devices, a bias was applied to the top electrode while the bottom electrode was grounded using a Keithley 4200 semiconductor parameter analyzer under air atmosphere.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

Acknowledgements

B.C.J. and Y.N. contributed equally to this work. This research was supported by the Global Frontier Center for Advanced Soft Electronics (2011-0031640 and 2011-0031638), the Creative Research Program of the ETRI (17ZB1300), and Nano-Material Technology Development Program of the National Research Foundation, Korea (2016M3A7B4905609).

Conflict of Interest

The authors declare no conflict of interest.

Keywords

amorphous In-Zn-Sn-O (a-IZTO), flexible selectors, memristor crossbar arrays, nonvolatile logic-in-memory circuits, surface electron accumulation layers (SEAL)

Received: August 17, 2017
Revised: October 1, 2017
Published online: November 23, 2017

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