Microelectronic Engineering 253 (2022) 111676

Contents lists available at ScienceDirect

Microelectronic Engineering

journal homepage: www.elsevier.com/locate/mee

Research paper

Improving the electrical performance of vertical thin-film transistor by engineering its back-channel interface

Kwang-Heum Lee [a], Seung Hee Lee [a], Sang-Joon Cho [b], Chi-Sun Hwang [c], Sang-Hee Ko Park [a,*]

[a] Department of Materials Science and Engineering, Korea Advanced Institute of Science and Technology, Daejeon 34141, Republic of Korea
[b] Park Systems, Corp., KANC 15F, Gwanggyo-ro 109, Suwon 16229, Republic of Korea
[c] Electronics and Telecommunications Research Institute, Daejeon 34129, Republic of Korea

ARTICLE INFO

Keywords:
Oxide semiconductor
Vertical thin-film transistor
Back-channel
Surface morphology

ABSTRACT

This paper reports the effect of the properties of a back-channel region of a vertical thin-film transistor (VTFT) on its electrical performance. The deposition of a thin layer of SiO_2 on a damaged back-channel region was found to improve the subthreshold swing (SS) from 0.25 to 0.12 V/dec, while maintaining the field-effect mobility. Detailed analysis of the surface morphology of the back-channel region revealed that the application of advanced photolithography resulted in a significantly smoother back-channel interface, yielding higher-performing VTFTs. The VTFT fabricated using a high-resolution, stepper photolithography system exhibited a linear mobility (μ_{lin}) of 14.60 cm^2/Vs, a saturation mobility (μ_{sat}) of 23.69 cm^2/Vs, and an SS value of 0.13 V/dec. Meanwhile, the VTFT fabricated using a standard projection aligner displayed μ_{lin}, μ_{sat}, and SS values of 5.74 cm^2/V·s, 13.87 cm^2/V·s, and 0.27 V/dec, respectively. These results revealed the electrical performance of the VTFT to be strongly influenced by the properties of the back-channel region.

1. Introduction

[1]Modern technologies such as virtual reality, augmented reality, and hologram displays are receiving considerable attention for the exploration of display devices and for various related industrial applications [1]. To offer high image quality in systems based on these technologies, exceptionally high resolution must be achieved.

As these applications are typically realized on a mobile display, minimizing the footprint of thin-film transistors (TFTs) is considerably desired. Several strategies have been reported to downscale TFTs, including design change [2,3] and nanoscale lithography [4]. The use of a vertical TFT (VTFT), which uses a vertical channel structure for size reduction, is a promising approach among them because the reduction of channel area is quite effective for the down-scaling of TFT while using a conventional photo-lithography process. Y. Uchida et al. proposed this VTFT structure in 1984, which was based on the amorphous silicon technology [5]. In the beginning of the study on VTFT, its usefulness of realizing nanoscale short-channel length without the limitation of photo-lithography process was mainly focused [5,6]. However, as the higher resolution was required along with the development of display technology, the size efficiency of VTFT received attention from researchers. For instance, I. Chan et al. mentioned higher device packing densities achievement by VTFT structure in their report, and conducted research on the reliability improvement of VTFT fabrication process [7].

Since the invention of In-Ga-Zn-O (IGZO) oxide semiconductor by Hosono et al. in 2003, there has been a lot of effort to introduce the oxide TFT to the display industry [8]. The outstanding performance of oxide TFT compared to the conventional a-Si:H TFT was highly attractive to the researchers and thought to be a key technology for the future display. Furthermore, the a-Si:H could be mostly formed by PECVD method, while various deposition methods were feasible for the oxide semiconductor. Especially the atomic layer deposition (ALD) offered the superior step coverage which was adequate for the reliable fabrication of VTFT. Advances have been demonstrated in oxide-semiconductor VTFTs [9–14]; however, their electrical characteristics are lower than those of planar TFTs. During VTFT fabrication, dry-etching is conducted on a

* Corresponding author.
E-mail address: shkp@kaist.ac.kr (S.-H.K. Park).

[1] vertical thin-film transistor, VTFT; sub-threshold swing, SS; thin-film transistors, TFTs; indium-tin-oxide, ITO; direct-current, DC; plasma-enhanced chemical vapor deposition, PECVD; plasma-enhanced atomic layer deposition, PEALD; gate insulator, GI; transmission electron microscopy, TEM; scanning electron microscopy, SEM; 3D atomic force microscopy, 3D-AFM; back-channel passivation, BCP; back-channel-passivated VTFT, BCP-VTFT; High resolution, HR; low resolution, LR

https://doi.org/10.1016/j.mee.2021.111676

Available online 3 December 2021

back-channel region of spacer, thereby generating defects. Thus, the effect of defects in the back-channel on the degradation of VTFT performance must be considered. Despite the phenomena of charge-trapping induced by defect generation [15,16] and carrier scattering due to interfacial roughness [17], there has been no detailed investigation into the formation of defects on the VTFT back-channel region. Therefore, further research on this aspect is essential for the improvement of the electrical performance of VTFTs.

In this study, the back-channel interface was modified to show that its properties affect the electrical characteristics of the VTFTs. Through both structural and electrical analyses, it was verified that back-channel interface engineering involving the passivation of the damaged surface or the fabrication of a smoother interface greatly improved the electrical performance of VTFTs.

2. Materials and methods

A top-gate, bottom-contact VTFT was fabricated as illustrated in Fig. 1. A 150-nm-thick, indium-tin-oxide (ITO), drain electrode was first formed on a thermally oxidized Si wafer by radio-frequency-superimposed direct-current (DC) sputtering, and patterned by dry-etching in a Cl_2/Ar gas mixture. A 500-nm-thick, silicon dioxide (SiO_2) spacer was deposited atop this electrode by plasma-enhanced chemical vapor deposition (PECVD) in an ambient gas mixture of SiH_4/N_2O at 300 °C. A top ITO layer, which served as the source electrode, was coated on the spacer; these ITO-SiO_2 stacked films were then sequentially dry-etched with a photoresist mask over the top electrode. SiO_2 dry-etching was performed in a CF_4/Ar gas mixture. This was followed by the deposition of a 5-nm-thick indium oxide (InO_x) active layer by plasma-enhanced atomic layer deposition (PEALD) involving a diethyl[bis(trimethylsilyl)amido]indium precursor and gaseous oxygen, along with an in-situ, O_2 plasma treatment of the substrate in the PEALD chamber to control the carrier concentration of InO_x. A 15-nm-thick layer of aluminum oxide (Al_2O_3) was then deposited by PEALD using a trimethylaluminum precursor and O_2 gas at 200 °C, where the Al_2O_3 film serves as an active protection layer (PL). The protection layer (PL) was adopted to our VTFT to preserve the surface of the active layer [18]. The InO_x active layer could be easily damaged by exposure to chemicals during the photolithography process. The Al_2O_3 protection layer could endure this chemical environment and avoid defect creation on the surface. Furthermore, the protected surface of the active layer act as a front channel, which is a main current path controlled by a gate-field, so the defect formation at this region is directly related to the overall performance of our device. Subsequently, the InO_x/Al_2O_3 stacked films were patterned with 300:2 dilute hydrofluoric acid, after which a 20-nm-thick Al_2O_3 second gate insulator (GI) was deposited on it by PEALD. A 100-nm-thick Mo gate was formed by DC sputtering and patterned by dry-etching in a Cl_2/O_2 gas mixture. Finally, a 100-nm-thick SiO_2 passivation layer was deposited by the PECVD process at 200 °C, marking the end of the fabrication step. This was followed by subjecting the transistor to a post-annealing process at 200 °C in a vacuum furnace.

For a back-channel passivation process analysis, we fabricated samples with vertically dry-etched SiO_2 spacer. An interfacial layer of Al_2O_3 was deposited by ALD, followed by a SiO_2 back-channel passivation film deposition by PEALD. The ALD Al_2O_3 layer was inserted in these analysis samples to distinguish the spacer and the back-channel passivation film because both films are consisted of SiO_2. Therefore, this Al_2O_3 layer was not adopted to the back-channel passivation process on the VTFTs.

All the electrical properties of the VTFT were measured using a semiconductor parameter analyzer (HP 4156C) at room temperature. Device structure and film morphology were analyzed with scanning electron microscopy (SEM; SU-5000, Hitachi), transmission electron microscopy (TEM; JEM-2100F HR and JEM-ARM200F, JEOL), and 3D atomic force microscopy (3D-AFM; NX-3DM, Park Systems).

3. Results and discussions

To investigate the effect of back-channel properties on the electrical characteristics of the VTFT, two different approaches were examined. The first involved passivating the surface of the spacer sidewall (Fig. 2 (a)), which was extensively damaged by dry-etching during the development of the vertical structure. This was carried out by deposition of a 3-nm-thick SiO_2 layer which was formed by PEALD at 300 °C, using bis-diethylaminosilane and O_2 gas as the Si precursor and reactant, respectively. Dry-etching in the absence of photoresist was performed to remove the SiO_2 film from the surface contact region of the electrodes. (Fig. 2(b)); this process is called back-channel passivation (BCP). Figs. 2 (c)–(e) show the TEM analysis results of the BCP process conducted on a test sample. During SiO_2 dry-etching, ions in the plasma are vertically accelerated toward the substrate because of the applied bias, physically etching the film. Simultaneously, the surface-fluorocarbon layer formed in the CF_4 plasma is removed from the horizontal region by ion bombardment, while it remains on the vertical sidewall and inhibits further reaction [7,19]. Therefore, the newly deposited SiO_2 film on the vertical region was observed to nearly maintain its thickness; this led to the film surface of the back-channel region getting covered by newly deposited SiO_2 and being less damaged from dry-etching compared to the initial spacer sidewall.

This process was applied to the fabrication of a VTFT, as a result of which a back-channel-passivated VTFT (BCP-VTFT) was obtained as shown in Fig. 3(a). The electrical characteristics of BCP-VTFT were compared with those of a non-passivated, reference VTFT. The channel width (W) and length (L) of the test and reference VTFTs were 8 and 0.5 μm, respectively. The most evident change was observed in the SS value (computed as $SS = dV_{gs}/d\log I_{ds}$, where V_{gs} is the gate voltage and I_{ds} is the drain current), as shown in Fig. 3(b). The BCP-VTFT exhibited a SS value of 0.12 V/dec, which was much lower than that of the reference VTFT (0.25 V/dec). The SS value is related to the bulk and interface trap density [20]. Because the fabrication conditions of the active layer and the GI were identical for both VTFTs, we attributed the difference in the

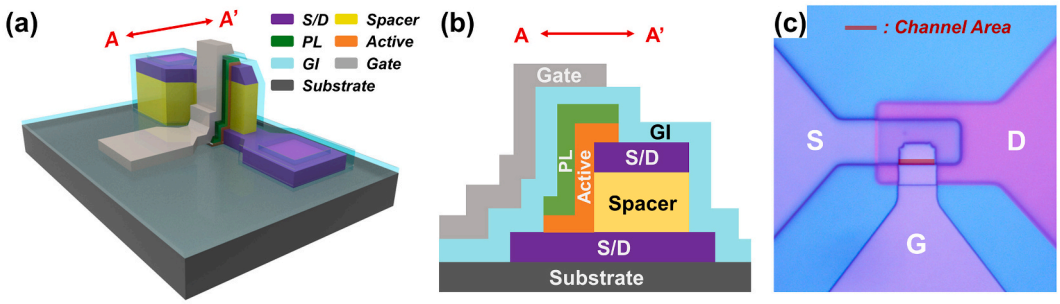

Fig. 1. (a) Schematic of VTFT. (b) Cross-section of the device through the A–A' direction. (c) Optical microscopic image of VTFT. The red bar indicates the channel area.

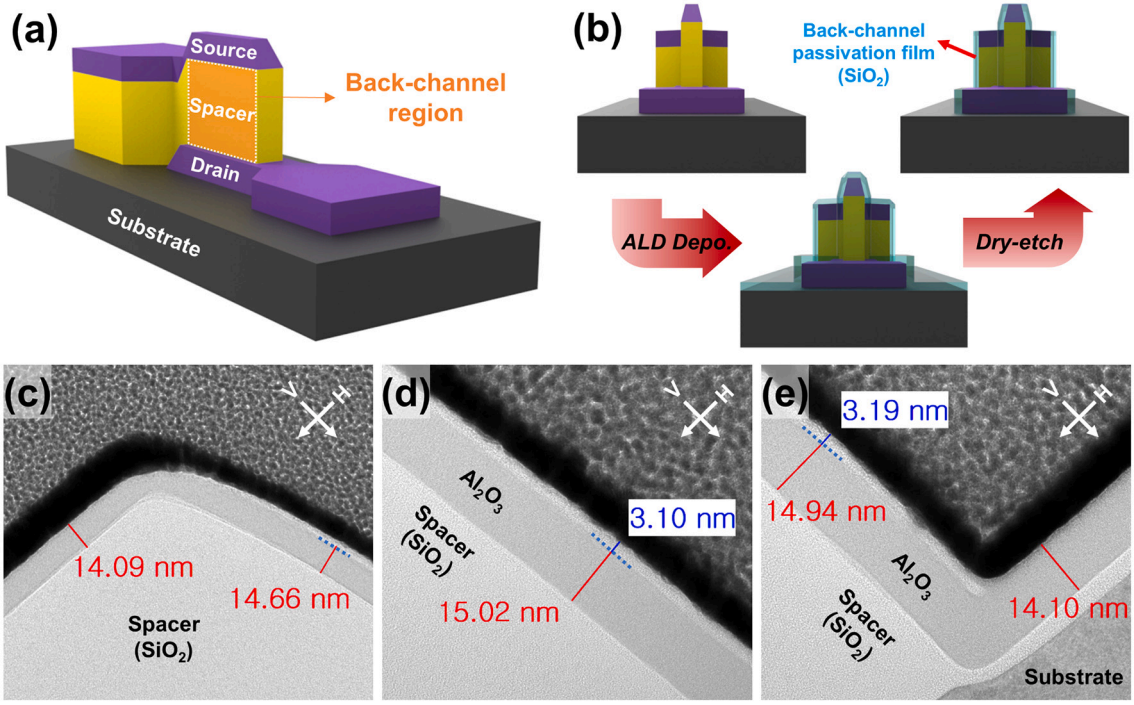

Fig. 2. Schematic of (a) back-channel region on spacer, (b) sequence of steps involved in back-channel passivation. TEM image of the test pattern representing the (c) top, (d) middle, and (e) bottom positions of the spacer. Arrows in the top-right corner correspond to the vertical (V) and horizontal (H) orientations relative to the substrate.

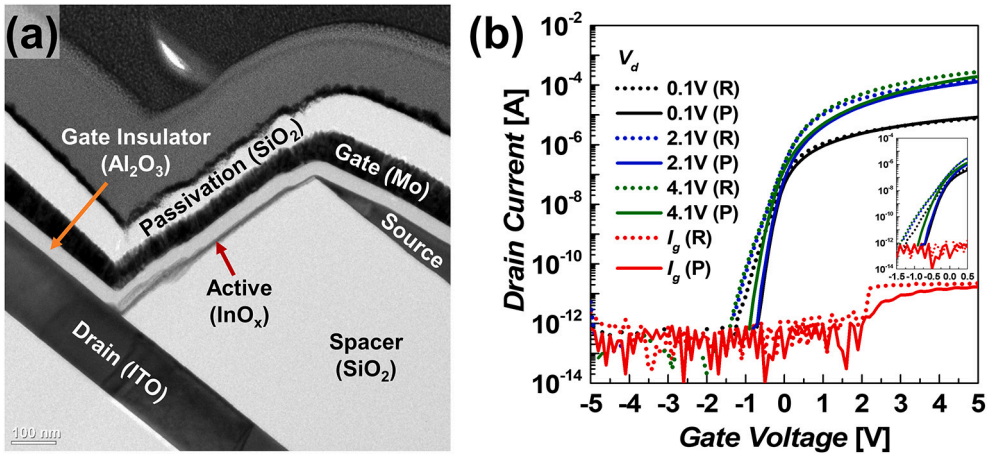

Fig. 3. (a) TEM image of the BCP-VTFT. (b) Transfer curves of the reference (R) and the BCP (P) VTFTs. The inset shows the transfer curve enlarged at the sub-threshold region.

SS value to the presence of defect states in the back-channel interface. A previous report on double-gate, oxide TFTs supports this idea of back-channel trap density influencing the SS value [15]; this influence is expected to be more dominant in the VTFTs described herein because of the thinness of the active layer and the large field-effect from the high-k GI film.

Although the SS value was improved by the BCP process, linear mobility showed no significant improvement and remained below 7 $cm^2/V{\cdot}s$, similar to that of the reference VTFT. However, since previous works have reported that InO_x, planar TFTs exhibit field-effect mobility of over 20 $cm^2/V{\cdot}s$ [21,22], the back-channel passivated VTFT in this study was believed to have a field-effect mobility suppressed by other factors at play. In Fig. 3(a), the back-channel interface is found to be uneven (implying higher roughness) when compared to other regions. It is well-known that the roughness of back-channel interface is strongly correlated to the electrical performance of the TFT because of carrier scattering [17]. Therefore, it is necessary to have a back-channel region with a smoother interface in order to improve the performance of the VTFT.

Considering this point, our second approach was to improve the surface morphology of the spacer sidewall through the advanced photolithography process. Fig. 4 presents SEM images of the spacer sidewall obtained from both high and low-resolution photolithography (HR, LR) systems. The HR process, using a stepper photolithography tool, yielded a steeper taper angle at the edge of the photoresist mask than the LR process, which used a standard projection aligner, did. Therefore, we can reduce the photoresist edge degradation that occurs during dry-etching due to the bombardment of vertically energetic ions, resulting in less line edge roughness (LER) [23] and deformation of photoresist pattern. This was transferred to the underlying spacer

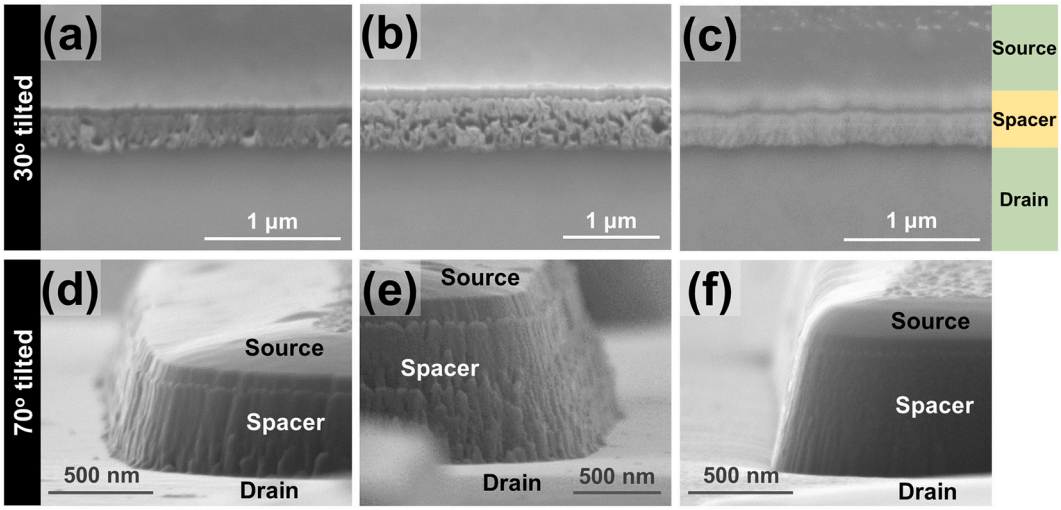

Fig. 4. SEM results of the spacer sidewall with images from (a), (d) LR-processing (b), (e) LR-processing with 1-μm-thick spacer, and (c), (f) HR-processing.

sidewall due to the characteristic of dry-etching method [24]. Accordingly, the sample from the HR method exhibited a smooth surface, while that from the LR method revealed a rougher surface with larger numbers of defect and/or scattering sites. The decline in surface morphology was more pronounced for the 1-μm-thick spacer sample as shown in Fig. 4(f), which might be related to its longer etch time.

Three types of VTFTs were fabricated with these samples and their transfer characteristics were analyzed as illustrated in Fig. 5. The channel width (W) was 8 μm for all VTFTs, while the channel length (L) was 0.5 μm for those in Fig. 5(a), (c), and 1 μm for that in Fig. 5(b). The electrical parameters extracted have been listed in Table 1. Both the linear mobility (μ_{lin}) and the saturation mobility (μ_{sat}) stands for the field-effect mobility measured from the linear and saturation mode of TFT operation regions, which are divided at a pinch-off point. μ_{lin} and μ_{sat} values were calculated from the value of maximum transconductance ($\mu = Lg_m/(WC_{ox}V_{ds})$, where g_m and C_{ox} refer to the transconductance and capacitance of the GI per unit area, respectively) at V_{ds} = 0.1 V and 4.1 V. The turn-on voltage (V_{on}) was extracted as the gate voltage (V_{gs}) corresponding to an I_{ds} of $(W/L) \times 10$ pA at $V_{ds} = 0.1$ V during the forward sweep. As shown in Table 1, the HR-VTFT exhibited the best performance, comparable to that of the InO_x planar TFT. In contrast, ineffectual values were obtained from the LR-VTFT with a 1-μm-thick spacer, which also exhibited a non-linear correlation between the I_{ds} and the channel length. The main and the only difference among these three devices was the surface morphology of spacer sidewall. Thus, we could draw a conclusion that a smoother roughness of spacer sidewall resulted better electrical performance of VTFT device.

Table 1
Variation of electrical characteristics of VTFTs with fabrication methods.*

Device	SS (V/dec)	V_{on} (V)	Hys. (V)	μ_{lin} ($cm^2/V{\cdot}s$)	μ_{sat} ($cm^2/V{\cdot}s$)
LR-VTFT	0.24	−0.8	0.1	6.24	8.33
LR-VTFT (1-μm spacer)	0.25	−0.6	0.2	3.52	6.78
HR-VTFT	0.13	−0.4	0.1	14.60	23.69

* **SS**: sub-threshold swing, $\boldsymbol{V_{on}}$: turn-on voltage, **Hys.**: hysteresis, $\boldsymbol{\mu_{lin}}$: linear mobility, $\boldsymbol{\mu_{sat}}$: saturation mobility.

$$SS = \frac{k_B T}{q}\left(1 + \frac{q^2 N_t}{C_{ox}}\right) ln(10) \quad (1)$$

The total trap density (N_t) was extracted from the SS value in Table 1, using Eq. (1) under the assumption of a uniform bulk-trap density, where k_B, T, and q are the Boltzmann constant, temperature, and elemental charge, respectively [25]. The resultant N_t values were 3.64 × 10^{12}, 3.84 × 10^{12}, and 1.42 × 10^{12} cm^{-2} eV^{-1} for the LR-VTFT, LR-VTFT (with the 1-μm spacer), and HR-VTFT, respectively. Compared to the two LR-VTFTs, the HR-VTFT exhibited much lower N_t value as shown in Fig. 6. All of these electrical parameters are consistent with the trend in Fig. 4, which explains the strong relationship between the surface morphology of the spacer sidewall and the electrical characteristics of the VTFT.

Finally, the surface profile of the back-channel region was verified through 3D-AFM conducted on the source-spacer-drain stacked samples

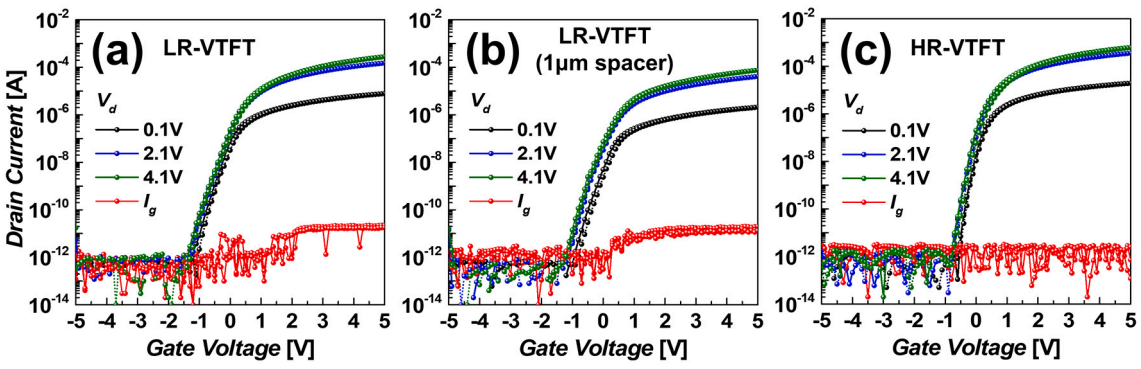

Fig. 5. Transfer curves of the (a) LR-VTFT, (b) LR-VTFT (with 1-μm spacer), and (c) HR-VTFT for drain voltages (V_{ds}) of 0.1, 2.1, and 4.1 V. The red line indicates the gate leakage current.

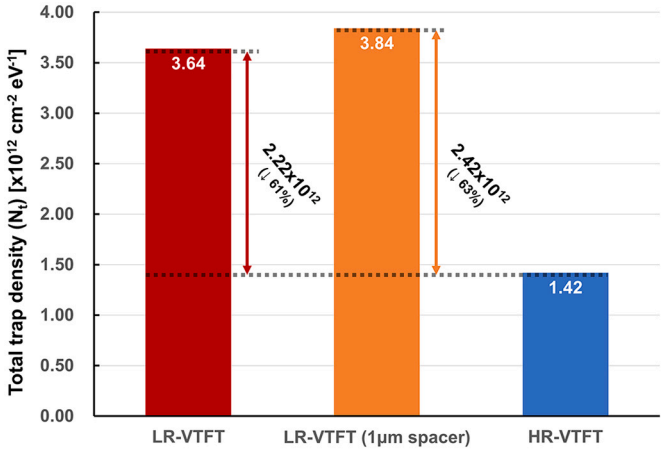

Fig. 6. Comparison of total trap density (N_t) values of LR-VTFT, LR-VTFT (1-μm spacer), and HR-VTFT, respectively.

fabricated under the same conditions used for the fabrication of the three VTFTs. This new AFM technology works with a tilted AFM head (Fig. 7(b)) and software correction to acquire an accurate vertical surface morphology and 3D-rendering images. Fig. 7(c) and Fig. 7(d) shows the analysis positions and 3D-renderings reconstructed from the AFM results, while the parameters extracted from AFM are summarized in Fig. 7(e). Similar to the results from the SEM images (Fig. 4), the HR-VTFT sample exhibited the smallest root-mean-square (RMS) value of sidewall roughness (SWR) while the top and bottom sidewall angles (SWAs) were the largest among the three samples. This result also supports our previous explanation of the relationship between the photolithography process and our dry-etching conditions, as illustrated in Fig. 7. Therefore, it was concluded that the steeper taper angle of photoresist formed by a high-resolution, stepper-based photolithography process helped reduction of damage from the dry-etching process and offered smoother back-channel morphology, resulting in improved electrical characteristics for the VTFT.

Compared to the previous reports, the HR-VTFT exhibited an outstanding electrical performance. The field-effect mobility was improved to be at least 2 times higher than the previous works, and the SS value was the lowest among them. Low off-current and gate leakage current, on/off ratio greater than 10^7, and turn-on voltage near zero were also obtained from our VTFT. Furthermore, these electrical parameters are even comparable to those of conventional planar TFTs, which means that much higher current drivability with nanoscale channel length and smaller footprint can be additionally achieved by the VTFT structure. From this result, we believe that the integration of high performance VTFT to a future generation display will be a step closer to reality.

4. Conclusions

This study investigated the effects of the properties of the back-channel of an InO_x VTFT on its electrical characteristics. The BCP process was found to improve SS values while maintaining field-effect mobility. The enhancement of the overall performance was attributed to the advanced photolithography process used for the spacer dry-etching; this could be attributed to the mechanism of the anisotropic dry-etching process. A high-resolution, stepper-based, photolithography process offered steeper taper angle of the photoresist, which yielded smoother back-channel surfaces owing to the dry-etching process. The vertical sidewall morphology analyzed by 3D-AFM confirmed the relationship between the patterning process and surface roughness. From these results, a minimally damaged, smooth back-channel interface was found to be instrumental in the realization of high-performance VTFTs. We hope that our study on the performance improvement of VTFT will provide useful insight to other researchers and be helpful for the realization of the next-generation display technology.

Funding

This work was supported by "The Cross-Ministry Giga KOREA Project" grant funded by the Korean government (MSIT) (1711073921,

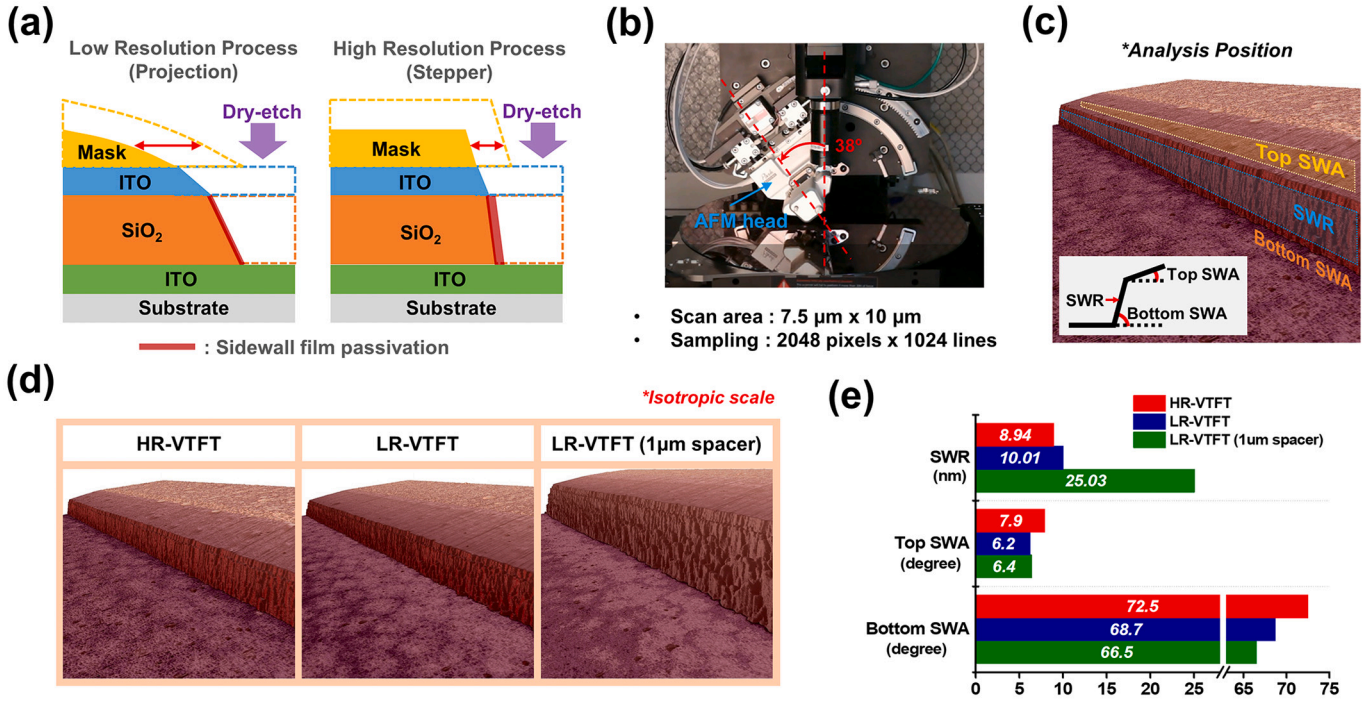

Fig. 7. Schematic diagram of (a) dry-etching mechanism for LR and HR-processes, (b) 3D-AFM conducted for sidewall profile measurement (c) analysis position for RMS SWR, top and bottom SWAs (d) 3D rendering of HR-VTFT, LR-VTFT, and LR-VTFT (1 μm spacer) samples, and (e) comparison of SWR, top, and bottom SWAs.

Development of Telecommunications Terminal with Digital Holographic Table-top Display); National Research Foundation of Korea (NRF) grant funded by the Korean government (MSIT) (2018R1A2A3075518); and LG Display.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

References

[1] Z. He, X. Sui, G. Jin, L. Cao, Progress in virtual reality and augmented reality based on holographic display, Appl. Opt. 58 (2019) A74–A81, https://doi.org/10.1364/AO.58.000A74.
[2] J.H. Choi, J.-H. Yang, J.-E. Pi, C.-Y. Hwang, Y.-H. Kim, G.H. Kim, H.-O. Kim, C.-S. Hwang, The new route for realization of 1-μm-pixel-pitch high-resolution displays, SID Symp. Dig. Tech. Papers. 27 (2019) 487–496, https://doi.org/10.1002/jsid.821.
[3] H.S. Lee, S. Jang, H. Jeon, B.-S. Choi, S.H. Cho, W.T. Kim, K. Song, H.Y. Chu, S. Kim, S.-C. Jo, J. Kwag, Large-area ultra-high density 5.6 10Kx6K 2250 ppi display, IEEE Electron Device Lett. 49 (2018) 607–609, https://doi.org/10.1002/sdtp.12409.
[4] S. Katsui, H. Kobayashi, T. Nakagawa, Y. Tamatsukuri, H. Shishido, S. Uesaka, R. Yamaoka, T. Nagata, T. Aoyama, K. Nei, Y. Okazaki, T. Ikeda, S. Yamazaki, A 5291-ppi organic light-emitting diode display using field-effect transistors including a c-axis aligned crystalline oxide semiconductor, J. Soc. Inf. Disp. 27 (2019) 497–506, https://doi.org/10.1002/jsid.822.
[5] Y. Uchida, Y. Nara, M. Matsumura, Proposed vertical-type amorphous-silicon field-effect transistors, IEEE Electron Device Lett. EDL-5 (1984) 105–107, https://doi.org/10.1109/EDL.1984.25849.
[6] H. Okada, Y. Uchida, K. Arai, S. Oda, M. Matsumura, Vertical-type amorphous-silicon MOSFET ICs, IEEE TED. 35 (1988) 919–922, https://doi.org/10.1109/16.3345.
[7] I. Chan, A. Nathan, Amorphous silicon thin-film transistors with 90° vertical nanoscale channel, Appl. Phys. Lett. 86 (2005), 253501, https://doi.org/10.1063/1.1949721.
[8] K. Nomura, H. Ohta, K. Ueda, T. Kamiya, M. Hirano, H. Hosono, Thin-film transistor fabricated in single-crystalline transparent oxide semiconductor, Science 300 (2003) 1269–1272, https://doi.org/10.1126/science.1083212.
[9] H.-I. Yeom, G. Moon, Y. Nam, J.-B. Ko, S.-H. Lee, J. Choe, J.H. Choi, C.-S. Hwang, S.-H.K. Park, Oxide vertical TFTs for the application to the ultra high resolution display, SID Symp. Dig. Tech. Papers. 47 (2016) 820–822, https://doi.org/10.1002/sdtp.10799.
[10] C.-S. Hwang, S.-H.K. Park, H. Oh, M.-K. Ryu, K.-I. Cho, S.-M. Yoon, Vertical channel ZnO thin-film transistors using an atomic layer deposition method, IEEE Electron Device Lett. 35 (2014) 360–362, https://doi.org/10.1109/LED.2013.2296604.
[11] Y.-M. Kim, H.-B. Kang, G.-H. Kim, C.-S. Hwang, S.-M. Yoon, Improvement in device performance of vertical thin-film transistors using atomic layer deposited IGZO Channel and polyimide spacer, IEEE Electron Device Lett. 38 (2017) 1387–1389. LED.2017.2736000.
[12] H.-R. Kim, J.-H. Yang, G.-H. Kim, S.-M. Yoon, Flexible vertical-channel thin-film transistors using in-Ga-Zn-O active channel and polyimide spacer on poly(ethylene naphthalate) substrate, J. Vac. Sci. Technol. B 37 (2019), 010602, https://doi.org/10.1116/1.5082898.
[13] H.-R. Kim, M. Furuta, S.-M. Yoon, Highly robust flexible vertical-channel thin-film transistors using atomic-layer-deposited oxide channels and Zeocoat spacers on ultrathin polyimide substrates, ACS Appl. Electron. Mater. 1 (2019) 2363–2370, https://doi.org/10.1021/acsaelm.9b00544.
[14] X. Yin, S. Deng, G. Li, W. Zhong, R. Chen, G. Li, F.S.Y. Yeung, M. Wong, H.S. Kwok, Low leakage current vertical thin-film transistors with InSnO-stabilized ZnO channel, IEEE Electron Device Lett. 41 (2020) 248–251, https://doi.org/10.1109/LED.2019.2960883.
[15] C.-Y. Jeong, D. Lee, S.-H. Song, Properties of bottom and top channel interfaces in double-gate back-channel-etched amorphous indium-gallium-zinc oxide thin-film transistors, J. Vac. Sci. Technol. B. 33 (2015), 030603, https://doi.org/10.1116/1.4919234.
[16] B. Zhang, H. Li, X. Zhang, Y. Luo, Q. Wang, A. Song, Performance regeneration of InGaZnO transistors with ultra-thin channels, Appl. Phys. Lett. 106 (2015), 093506, https://doi.org/10.1063/1.4914296.
[17] J.F. Wager, B. Yeh, Chapter nine — oxide thin-film transistors: device physics, in: B.G. Svensson, S.J. Pearton, C. Jagadish (Eds.), Semiconductors and Semimetals, of Oxide Semiconductors vol. 88, Elsevier, 2013, pp. 283–315.
[18] S.-H.K. Park, D.-H. Cho, C.-S. Hwang, S. Yang, M.K. Ryu, C.-W. Byun, S.M. Yoon, W.-S. Cheong, K.I. Cho, J.-H. Jeon, Channel protection layer effect on the performance of oxide TFTs, ETRI J. 31 (2009) 653–659, https://doi.org/10.4218/etrij.09.1209.0043.
[19] G.S. Oehrlein, Y. Kurogi, Sidewall surface chemistry in directional etching processes, Mater. Sci. Eng. R. Rep. 24 (1998) 153–183, https://doi.org/10.1016/S0927-796X(98)00016-3.
[20] I.M. Choi, M.J. Kim, N. On, A. Song, K.-B. Chung, H. Jeong, J.K. Park, J.K. Jeong, Achieving high mobility and excellent stability in amorphous in-Ga-Zn-Sn-O thin-film transistors, IEEE TED. 67 (2020) 1014–1020, https://doi.org/10.1109/TED.2020.2968592.
[21] H.-I. Yeom, A study on high mobility indium oxide thin films and thin-film transistors by means of plasma-enhanced atomic layer deposition, M.S. thesis, Dept. of MSE, KAIST, Daejeon, Korea, 2016.
[22] H.-I. Yeom, J.B. Ko, G. Mun, S.-H.K. Park, High mobility polycrystalline indium oxide thin-film transistors by means of plasma-enhanced atomic layer deposition, J. Mater. Chem. C 4 (2016) 6873–6880, https://doi.org/10.1039/c6tc00580b.
[23] S.G. Yazgi, T. Ivanov, M. Holz, I.W. Rangelow, B.E. Alaca, Line edge roughness metrology software, JVST B. 38 (2020), 012602, https://doi.org/10.1116/1.5122675.
[24] D.P. Hamblen, A. Cha-Lin, Angular etching correlations from RIE: application to VLSI fabrication and process modeling, J. Electrochem. Soc. 135 (1988) 1816–1822, https://doi.org/10.1149/1.2096138.
[25] W. Cai, J. Wilson, J. Zhang, J. Brownless, X. Zhang, L.A. Majewski, A. Song, Significant performance enhancement of very thin InGaZnO thin-film transistors by a self-assembled monolayer treatment, ACS Appl. Electron. Mater. 2 (2020) 301–308, https://doi.org/10.1021/acsaelm.9b00791.