Buffer Layer Engineering of Indium Oxide Based Trench TFT for Ultra High Current Driving

Youngjun Im, Seong-In Cho, Jingyu Kim, Namgyu Woo, Jong Beom Ko, and Sang-Hee Ko Park

***Abstract*— Oxide thin-film transistors (TFTs) with high mobility that exceed 100 $cm^2/V{\cdot}s$ and appropriate turn-on voltage (V_{on}) are necessary to drive next-generation displays and memory devices. However, a trade-off relationship exists between mobility and V_{on}, making it difficult to achieve both in the same oxide TFT. In this letter, we propose a buffer layer engineered trench-TFT (T-TFT) as a solution to this trade-off problem. Planar-TFT (P-TFT) with an Al_2O_3 buffer layer exhibits a high current level; however, its V_{on} value is unsuitable. In contrast, P-TFT with an SiO_2 buffer demonstrates a V_{on} close to zero, although its mobility remains below 100 $cm^2/V{\cdot}s$. The T-TFT, which incorporates both Al_2O_3 and SiO_2 buffer layers, shows a high mobility of 129 $cm^2/V{\cdot}s$ and a suitable V_{on} of −0.4 V, selectively utilizing the advantages of P-TFTs. Based on electrical measurements and material analyses, the active layer on each buffer layer performs a distinct role in the T-TFT; the active layer on SiO_2 serves as the "V_{on} determiner," owing to its low oxygen vacancy, whereas the active layer on Al_2O_3 enhances the mobility, through reduced electron trap sites and a smooth surface.**

***Index Terms*— Buffer layer, indium oxide, trench structure, high mobility, thin-film transistors, PEALD.**

I. Introduction

OXIDE thin-film transistors (TFTs) are currently being studied extensively due to their ability to simultaneously exhibit high mobility, large-area uniformity, and a good on/off ratio [1]. They demonstrate high mobility characteristics that are over ten times greater than amorphous silicon (a-Si) TFTs (∼1 $cm^2/V{\cdot}s$). However, to drive next-generation displays such as extended reality (XR) and 8K displays, and semiconductor memory devices, higher performance TFTs with increased mobility are required. For this reason, low-temperature polysilicon (LTPS) is still used for driving TFTs in display and NAND flash devices, despite its high temperature and expensive manufacturing process [2]. Consequently, developing an oxide semiconductor with mobility of 100 $cm^2/V{\cdot}s$, a value comparable to LTPS, is considered a major objective in this field. Achieving such high mobility is challenging; moreover, the unique trade-off relationship between mobility and turn-on voltage (V_{on}) in oxide TFTs increases the difficulty [3], [4]. A high carrier concentration is required to achieve high mobility due to the energy barrier above the conduction band minimum. However, this result in a negative V_{on} and in extreme cases, the active layer loses its function as a semiconductor.

The buffer layer, placed beneath the active layer, can significantly influence the properties of the oxide semiconductors [5], such as atomic incorporation from buffer to the active layer and roughness of the buffer layer. Defect generation is also dominated by the material properties of the buffer layer. These effects determine the electrical properties of oxide TFTs. This effect is particularly crucial for plasma-enhanced atomic layer deposition (PEALD) processed high mobility oxide semiconductors, such as indium oxide (InO_x). A thin layer of InO_x is generally used owing to its high carrier concentration [6]. Moreover, the properties of oxide semiconductors deposited by PEALD are influenced by the underlying buffer layer; the PEALD process is governed by surface reactions [7]. Consequently, buffer layer engineering can be used to design high mobility oxide TFT with a proper V_{on} value.

In this letter, we developed an InO_x TFT with a high mobility of 129 $cm^2/V{\cdot}s$ and V_{on} close to 0 V by simultaneously controlling the buffer layers in terms of the material and structure. A new type of trench-TFT (T-TFT) was fabricated by allowing the active layer, deposited through PEALD, to simultaneously contact two types of buffer layers (SiO_2 and Al_2O_3). The trench structure is chosen to simultaneously contact the active layer and two buffer layers. The InO_x exhibits different conductivities depending on the underlying layer, and the T-TFT that selectively utilizes two buffer layers capitalized on each layer. We develop a T-TFT with a mobility that is more than twice as high as that of the conventional planar-TFT (P-TFT) while maintaining a V_{on} close to zero.

II. Experimental Section

Fig. 1(a) and (b) show the schematics of the fabricated T-TFTs and P-TFTs. Apart from the buffer layer process, subsequent processes were identical for T-TFTs and P-TFTs. For the T-TFT buffer layer, a 50 nm-thick Al_2O_3 layer

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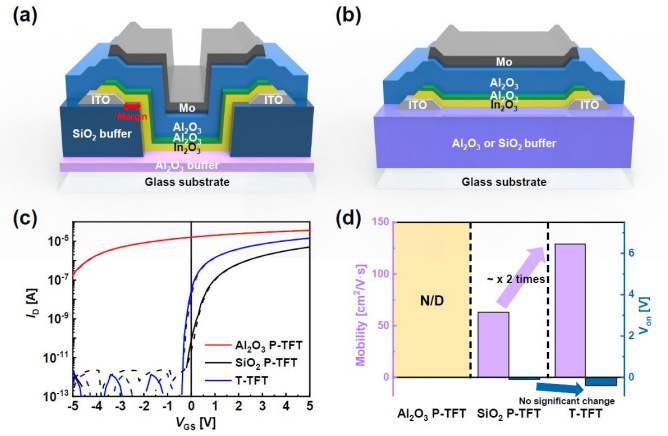

Fig. 1. Schematics of (a) T-TFT and (b) P-TFT. (c) Transfer curves of T-TFT and two P-TFTs (drain voltage = 0.1 V). The solid lines and dash lines show forward and backward sweep, respectively. (d) Comparison of the electrical properties of Al_2O_3 P-TFT, SiO_2 P-TFT, and T-TFT.

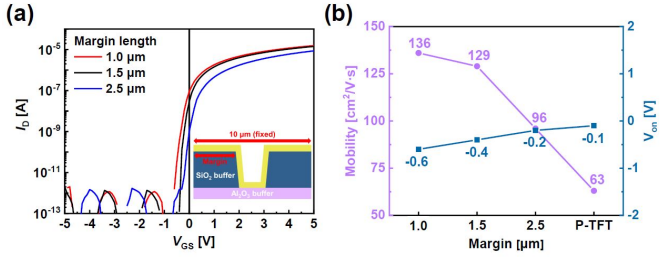

Fig. 2. (a) Transfer curves of T-TFTs with different lengths of margins: 1.0, 1.5, and 2.5 μm. (b) Mobility and V_{on} values of T-TFTs based on the margin length and SiO_2 P-TFT.

was deposited by thermal atomic layer deposition (ALD) at 200 °C, followed by the deposition of a 200 nm-thick SiO_2 by plasma-enhanced chemical vapor deposition (PECVD) at 300 °C. Next, SiO_2 was patterned by reactive ion etching using CF_4 gas, which exhibited etch selectivity between Al_2O_3 and SiO_2. For the P-TFT buffer layer, a single buffer layer (either Al_2O_3 or SiO_2) was deposited without etching. Next, a 150 nm-thick InSnO (ITO) was deposited by sputtering, as source/drain electrodes. InO_x, a high mobility oxide semiconductor, was deposited at a thickness of 5 nm using PEALD at 200 °C. To examine the effect of the buffer layer, the thickness of the semiconductor should be thin; however, it should still be able to demonstrate high mobility. Therefore, InO_x with a reduced thickness was chosen as the active layer. Then, the protection layer, which protects the active layer from the chemical was deposited on InO_x and simultaneously patterned together with InO_x [8]. Next, a gate insulator was deposited. Al_2O_3 for the protective layer (10 nm) and gate insulator (35 nm) were deposited by PEALD at 200 °C. Finally, a 150 nm-thick Mo was deposited for the gate electrode. Except for the buffer layer, all layers were patterned by photolithography and wet etching. The fabricated TFTs were exposed to vacuum annealing at 280 °C for 2 h.

The width and length of the active layer of the P-TFT were 20 and 10 μm, respectively, whereas those of the T-TFT were 20 and 10.4 μm, respectively, owing to the vertical part. In addition, the upper horizontal part of the active layer is referred to as the "margin." While the total channel length does not change as the margin length longer, the length of the active layer in contact with SiO_2 increase [9].

III. Results and Discussion

Fig. 1(c) shows the transfer curves of the T-TFT and two different types of P-TFTs. A comparison of the mobility and V_{on} of each TFT is shown in Fig. 1(d). The hysteresis of all TFTs reached zero. The P-TFT with an Al_2O_3 buffer layer exhibited a significant negative shift in its V_{on} value. However, by examining the shape of the transfer curve, it appeared to exist in an off-state at a gate voltage (V_{GS}) lower than −5 V, the semiconducting characteristics were still maintained. Although the mobility could not be extracted due to the highly negative V_{on}, the drain current (I_D) was quite high. Conversely, SiO_2 P-TFT demonstrated typical transfer characteristics, with a mobility of 63 $cm^2/V{\cdot}s$ and a V_{on} of −0.1 V. Although this device exhibited a mobility of less than 100 $cm^2/V{\cdot}s$, this device showed a proper V_{on} value even with relatively high mobility for oxide TFTs. Notably, all materials and processes were the same for the two types of P-TFTs, except for the buffer material, yet the electrical properties differed completely. The T-TFT, whose active layer was deposited on Al_2O_3 and SiO_2, exhibited significantly improved transfer characteristics compared with the P-TFT with an SiO_2 buffer layer. The T-TFT showed an outstandingly high mobility of 129 $cm^2/V{\cdot}s$, approximately twice as high as the P-TFT with an SiO_2 buffer layer. These electrical properties were extracted with a channel length of 10.4 μm, involving the InO_x on Al_2O_3. Moreover, V_{on} showed no significant difference (only 0.3 V). Based on these results, the Al_2O_3 buffer layer could enhance the mobility of the TFT, while the SiO_2 buffer layer contributed to maintaining V_{on} near zero.

To clarify the effect of each buffer layer, the electrical properties were measured and compared according to the length of the margin (Fig. 2). Regardless of the margin length, the total channel length of the TFT was fixed at 10 μm (top view; the actual channel length was 10.4 μm, including the vertical part), and the change in the margin length only influenced the length of each buffer layer in contact with InO_x. As the margin length increased from 1.0 to 2.5 μm, mobility decreased (from 136 to 96 $cm^2/V{\cdot}s$), whereas the V_{on} had a slight positive shift (from −0.6 to −0.2 V). This trend agreed with the results shown in Fig. 1(d). From the electrical parameters of P-TFTs and T-TFTs according to margin length, it can be confirmed that the SiO_2 and Al_2O_3 buffer layers improved the V_{on} and mobility, respectively.

The material property of InO_x on each buffer layer should be investigated to comprehend the electrical properties of T-TFTs. As reported, the properties of PEALD-processed semiconducting films depend on the substrate material [7]. Therefore, to analyze the bonding state of InO_x, the O1s peak from X-ray photoelectron spectroscopy (XPS) was examined (Fig. 3). From the deconvoluted O1s peak, more oxygen vacancies (V_o) were observed in InO_x on Al_2O_3 than on SiO_2. V_o is an electron donor in oxide semiconductors, which can boost mobility and shift V_{on} toward the negative [10], [11], [12].

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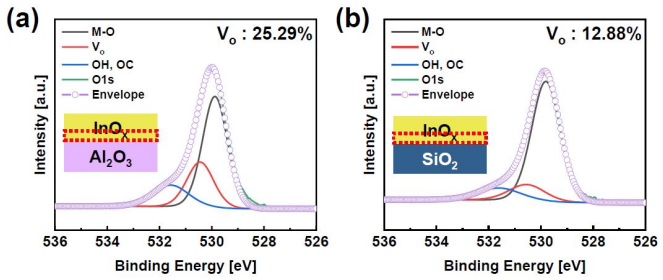

Fig. 3. Deconvoluted O1s peaks of InO_x on (a) Al_2O_3 and (b) SiO_2.

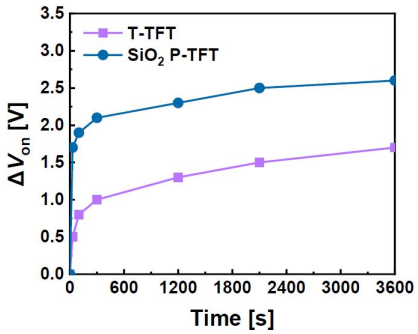

Fig. 4. PBTS stability of T-TFT and P-TFT with the SiO_2 buffer layer.

Consequently, this XPS results aligned with the electrical properties of the TFTs. For InO_x on Al_2O_3, high electron concentration owing to its high V_o concentration, result in high mobility and negative V_{on}. On the other hand, InO_x on SiO_2 exhibited a V_{on} close to 0 V due to its proper amount of electron from relatively low V_o. The differing conductance originated from the V_o is a primary reason for the observed differences in the electrical properties.

The number of electron trap sites according to the buffer layer should be considered. These trap sites impede electron flow, resulting in a degradation in mobility [4]. Positive bias temperature stress (PBTS) stability was measured to estimate the electron trap sites, as shown in Fig. 4. T-TFT (1.59 V) demonstrated better stability than P-TFT with SiO_2 buffer (2.49 V). This results from the high carrier concentration of InO_x on Al_2O_3. Free electrons in oxide semiconductors can passivate the trap sites, resulting in improved stability. For the T-TFT, InO_x on Al_2O_3 had fewer trap sites, thereby enhancing the stability of T-TFT. The high mobility in T-TFT also resulted from the fewer defects hindering electron flow.

The roughness of the buffer layer can be another factor that affects mobility [13]. This effect would be more significant in thin semiconductor films. Fig. 5 (a) and (b) show the surface profiles of Al_2O_3 and SiO_2, respectively, as measured by atomic force microscopy (AFM). SiO_2 showed a significantly rougher surface than Al_2O_3. The smooth surface of Al_2O_3 enhanced the mobility of InO_x owing to less surface scattering.

The distinct roles of InO_x on SiO_2 and Al_2O_3 are illustrated in Fig. 6. When a negative V_{GS} was applied, InO_x on SiO_2 existed in the off-state and the total channel became off-state. Therefore, the V_{on} of T-TFT could maintain a V_{on} close to 0 V and InO_x on SiO_2 acted as a "V_{on} determiner." Conversely, when a positive V_{GS} was applied, both InO_x on SiO_2 and Al_2O_3 turned on. In this state, InO_x on Al_2O_3 acted as a

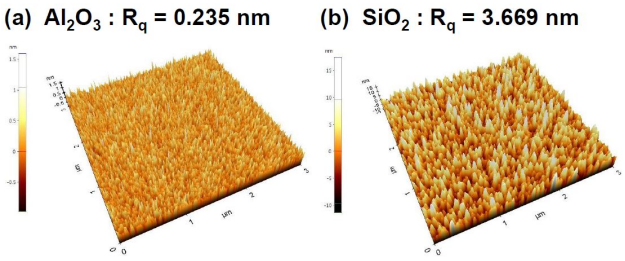

Fig. 5. 3D AFM images and their root-mean-square roughness (R_q) values of (a) Al_2O_3 and (b) SiO_2 buffer layer.

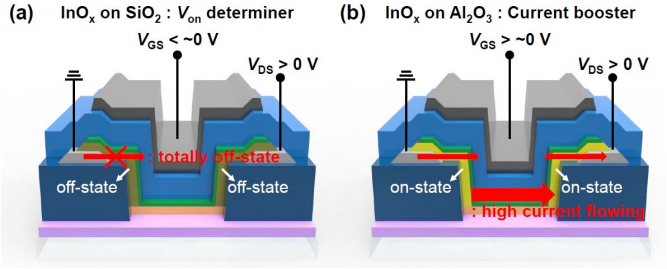

Fig. 6. Operating mechanism of T-TFT. The role of (a) InO_x on SiO_2 as V_{on} determiner, and (b) InO_x on Al_2O_3 as current booster.

"current booster" owing to its fewer trap sites, smooth surface and higher amounts of shallow donor of V_o. High mobility that exceeding 100 $cm^2/V{\cdot}s$ and a V_{on} close to 0 V were successfully achieved by separating the roles of InO_x on each buffer.

IV. Conclusion

In this letter, we developed oxide TFTs with high current driving ability and V_{on} close to 0 V through buffer layer engineered T-TFT for the first time. Al_2O_3 P-TFT showed an excessively negative V_{on}, although its I_D was quite high. On the other hand, SiO_2 P-TFT showed a proper V_{on} with lower mobility than 100 $cm^2/V{\cdot}s$. T-TFT which simultaneously used Al_2O_3 and SiO_2 buffer layers selectively capitalized on Al_2O_3 P-TFT and SiO_2 P-TFT. Based on the variation in margin length, these electrical properties were induced by the buffer layer. The InO_x on each buffer layer had different roles in the T-TFT. Owing to its low V_o concentration, InO_x on SiO_2 acted as a "V_{on} determiner," and maintained the V_{on} of T-TFT close to 0 V. Additionally, InO_x on Al_2O_3 performed as a "current booster," owing to its fewer trap sites and smooth surface. This buffer layer engineered T-TFT could be an excellent method of fabricating high current driving oxide TFTs with a proper V_{on} by resolving the trade-off relationship between mobility and V_{on}.

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