Effect of High Film Stress of Mo Source and Drain Electrodes on Electrical Characteristics of Al Doped InZnSnO TFTs

Jaehan Bae, Boo Soo Ma, Gukjin Jeon, Wooseok Jeong, Chang Han Je, Taek-Soo Kim, and Sang-Hee Ko Park

***Abstract*—We report how the intrinsic film stress of Mo source and drain (S/D) electrodes affects the electrical properties of Al doped InZnSnO thin-film transistors (TFTs). By controlling the Ar pressure during the sputtering process, Mo films with different film stresses (1948.2 MPa and 168.8 MPa) were formed. Two kinds of TFTs were fabricated applying these films as S/D electrodes. The TFTs made with the high-stress S/D showed linear mobility (μ_{lin}) of 29.44 cm^2 /Vs and hysteresis of 3.39 V while the TFTs with the low-stress S/D showed μ_{lin} of 35.25 cm^2 /Vs and hysteresis of 1.97 V. Under positive bias temperature stress (1 MV/cm, 60 °C, 3600 s), V_{on} was 4.48 V and 7.28 V for the TFTs with the low-stress S/D and high-stress S/D, respectively. X-ray photoelectron spectroscopy and finite element (FE) simulation results revealed that oxygen deficient sites in the active layer generated by the film stress of the Mo S/D induced degradation of the device characteristics.**

***Index Terms*—Al doped InZnSnO TFT, finite element simulation, oxygen vacancy, S/D film stress.**

I. Introduction

RECENTLY, explosive studies have been conducted on amorphous oxide thin-film transistors (TFTs), for they are regarded as promising devices to realize high resolution, large-screen display due to their high mobility, low fabrication temperature, scalability, and easy processing [1], [2]. Accordingly, numerous efforts have been made to achieve high performance oxide TFTs by optimizing the material selection, deposition method, and post-treatment, etc [3]–[5].

The effect of film stress, however, has not been extensively discussed in oxide TFT field. The film stress is an intrinsic property determined by the film deposition conditions such as pressure, bias, and type of sputtering gas [6]. In addition, even cracking and decohesion may occur when the film stress becomes severe. Therefore, it is important to obtain thin films having a good film quality while lowering the film stress in the large-screen display process. Also, even if no visible failure occurs, it has been reported that the device characteristics can be improved via film stress modulation in Si-based field-effect transistors [7]–[9]. Despite this importance, few people have reported a detailed description and specific mechanism of how film stress affects the device performance in the case of oxide TFTs. Therefore, the film stress would also be a noteworthy process variable and should be intensively investigated in the oxide TFT research.

Herein, we applied Mo films having different film stresses as the source and drain (S/D) electrodes of Al doped InZnSnO (Al-IZTO) TFTs, and compared their electrical characteristics. X-ray photoelectron spectroscopy (XPS) was used to investigate chemical state changes in the active layer. Finite element (FE) simulations provided the stress distribution in the actual device structure. The results revealed that the electrical properties of Al-IZTO TFTs can be degraded when the film stress of Mo S/D electrodes was high.

II. Experiment

Al-IZTO TFTs with a back-channel etched structure were fabricated on Si wafers with thermally grown 300-nm-thick SiO_2 (Fig. 1(a)). An 80-nm-thick layer of Mo deposited by DC sputtering at 3 mTorr of Ar pressure formed the gate electrode, and a 200-nm-thick SiO_2 gate insulator (GI) was deposited by plasma-enhanced chemical vapor deposition (PECVD) at 350 °C. Then, a 30-nm-thick Al-IZTO active layer was deposited by RF sputtering. Mo S/D electrodes (80-nm-thick) were deposited by DC sputtering at two different Ar pressures (0.1 mTorr and 5 mTorr) to control the film stress of the electrodes. The passivation layer of SiO_2 was formed by PECVD at 300 °C. Photolithography and wet etching were performed to define patterns of gate, active, S/D,

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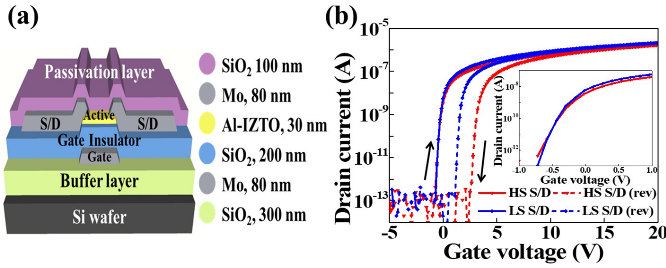

Fig. 1. (a) Schematic diagram of back-channel etched structure Al-IZTO TFT. (b) Transfer curves of Al-IZTO TFTs with S/D of different film stresses. Drain voltage (V_d) was set at 0.1 V, and gate voltage (V_g) swept from −5 V to 20 V (solid lines), then reversely swept from 20 V to −5 V (dashed lines). Inset shows the subthreshold region of transfer curves.

and passivation layers. The fabricated devices were post-annealed in a vacuum for 2 hours at 270 °C, which is lower than the deposition temperature of passivation layer in order to minimize the effects of hydrogen diffusion [10]. The channel width and length were 20 μm and 10 μm, respectively.

For film stress calculations, the curvature of the Si wafer before and after deposition of the 80-nm-thick Mo film was measured by FSM500TC stress gauge equipment. To obtain basic properties of Mo films, X-ray reflectometry (XRR) and atomic force microscopy (AFM) were performed by SmartLab X-ray diffractometer and XE-100 scanning probe microscope, respectively. Electrical characteristics of TFTs were measured by HP4156A semiconductor parameter analyzer. XPS analysis was conducted by using K-alpha XPS equipment, and an Ar ion (Ar^+) beam was used to etch the sample. For the FE analysis, a commercial software (ABAQUS v 6.14-1) was used to simulate stress distribution of the TFT structure.

III. Results and Discussion

The film stress values of the Mo thin films were calculated by the Stoney formula below:

$$\sigma = \frac{B_s d_s^2}{6 d_f}\left(\frac{1}{R} - \frac{1}{R_0}\right) \quad (1)$$

where σ is the film stress, and B_s is the biaxial modulus of the substrate. R_0 and R are the curvatures of the substrate before and after film deposition, respectively, and d_s and d_f are the respective thickness of the substrate and film. Herein, we used values of 180 GPa and 0.625 mm for B_s and d_s, respectively [11]. The calculated stress of Mo deposited at 0.1 mTorr (High-stress (HS) Mo) and 5 mTorr (Low-stress (LS) Mo) were 1948.2 MPa and 168.8 MPa, respectively. The positive values of both Mo layers indicate that they were under residual tensile stress. Fig. 1(b) shows the transfer curves of the post-annealed Al-IZTO TFTs using Mo S/D electrodes with different stresses. For each condition, all TFTs showed good uniformity with small standard deviation across 10 devices (Table I). When the HS S/D was used, linear mobility (μ_{lin}) decreased by 5.81 cm^2/Vs and hysteresis increased by 1.42 V while subthreshold swing (S.S) and turn-on voltage (V_{on}) showed little difference compared to those of TFTs made with the LS S/D.

In order to investigate the effect of other factors which may affect the electrical characteristics of TFTs, XRR and AFM were performed to obtain basic properties of HS and LS Mo films. Fig. 2(a) shows that the critical angle of HS Mo was larger than that of LS Mo, which indicates that the density of HS Mo was larger than that of LS Mo. According to the calculated results, the density of HS Mo and LS Mo were 9.92 g/cm^3 and 8.59 g/cm^3, respectively. Also, the AFM results (Fig. 2(b)∼(c)) show that root-mean square (RMS) roughness of HS Mo and LS Mo were 0.47 nm and 0.74 nm, respectively. In addition, the resistivity of HS and LS Mo films obtained through sheet resistance measurements were $1.86 \times 10^{-5}\Omega \cdot$ cm and $9.75 \times 10^{-5}\Omega \cdot$ cm, respectively. Considering other properties of Mo except the film stress, it was assumed that TFTs made with HS S/D show better device characteristics. The actual device performance, however, showed contradictory results. Therefore, we considered that negative effect of high film stress was dominant in degrading electrical characteristics of Al-IZTO TFTs.

TABLE I

Electrical Characteristics of Al-IZTO TFTs Made With HS S/D and LS S/D. Average and Standard Deviation Values of 10 TFTs at Each Stress Condition Are Shown. All Parameters Were Extracted From Measured Data During the Forward Sweep

	HS S/D	LS S/D
μ_{lin} (cm^2/Vs)	29.44±1.65	35.25±1.58
Hysteresis (V)	3.39±0.26	1.97±0.21
S.S (V/dec)	0.23±0.02	0.21±0.02
V_{on} (V)	-0.51±0.07	-0.58±0.09

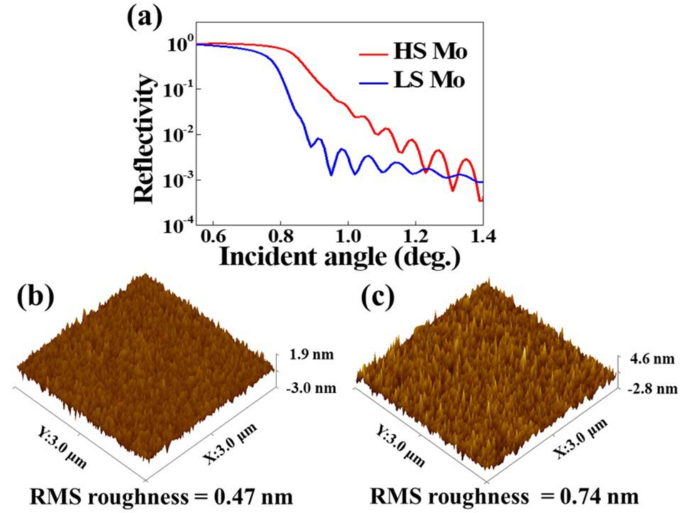

Fig. 2. (a) Reflectivity curve of HS Mo and LS Mo. AFM images of (b) HS Mo, (c) LS Mo.

XPS analysis was conducted to investigate the chemical states in the bulk region of the Al-IZTO layer after deposition of the Mo having different stresses. The chemical state of the Al-IZTO without Mo deposition was also observed for reference. Fig. 3(a)∼(c) present the oxygen 1s (O1s) peak of the Al-IZTO without Mo deposition, after LS Mo deposition, and after HS Mo deposition, respectively. Samples used for analysis had the same stacking as the TFT (insets of Fig. 3(a)∼(c)). The O1s peak was deconvoluted

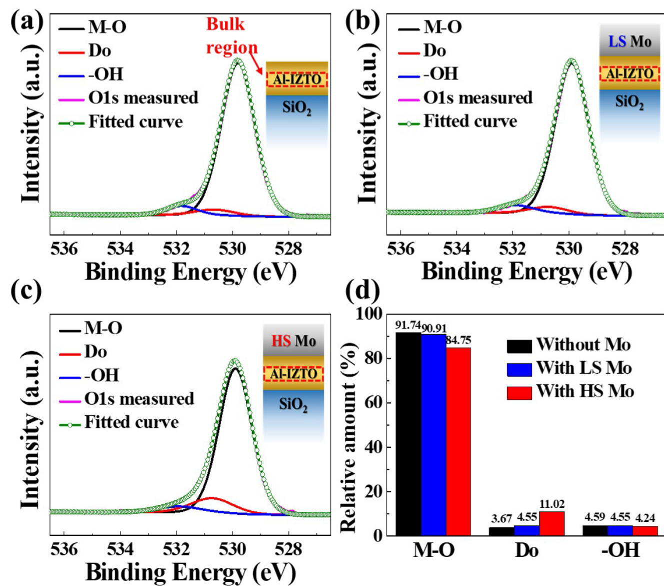

Fig. 3. O1s peak in the bulk region of Al-IZTO layer (a) without Mo deposition, (b) after LS Mo deposition, (c) after HS Mo deposition. (d) Relative amounts of M-O, D_o, -OH in the bulk region of Al-IZTO layer in each case.

into three sub-peaks corresponding to metal-oxygen bonds (M-O, 529.85 $\pm$ 0.05 eV), oxygen deficiency (D_o, 530.69 $\pm$ 0.05 eV), and oxygen-hydrogen bonds (-OH, 531.87 $\pm$ 0.05 eV) [12]. As shown in Fig. 3(d), when HS Mo was deposited, M-O decreased by 6.99 % and D_o increased by 7.35 % in the Al-IZTO compared with the case without Mo deposition. In contrast, the change in amount of M-O and D_o was less than 1 % when LS Mo was deposited.

Because identical materials were used, we speculated that the difference in the physical stress of Mo caused the observed change in the O1s peak of the Al-IZTO. Also, the film stress of the 30-nm-thick Al-IZTO calculated by (1) was 209.1 MPa, which was slightly greater than that of the LS Mo. Therefore, it is inferred that the LS Mo did not apply enough physical stress to affect the Al-IZTO layer, while the HS Mo generated sufficient stress to break metal-oxygen bonds and increase the number of oxygen-deficient sites.

Fig. 4(a) and (b) show images of stress distribution in the actual TFT structure simulated by the FE analysis. The cross-section of the TFT was modeled as a deformable 2D shell, and the measured film stresses estimated by (1) were applied to each layer as a pre-defined field. As shown in Fig. 4, the applied stress on the active layer increased when the stress of the S/D was high. Also, the calculated strain of the active layer were 0.59 % and 0.12 % when HS S/D and LS S/D were used, respectively. Compared with previous studies, it is evident that the HS S/D induced sufficient strain on the active layer to affect device characteristics [13].

Considering the results of XPS and FE analysis comprehensively, it is inferred that higher film stress of S/D electrodes led to larger strain in the active layer, and the resulting increase in oxygen deficient sites degraded the device characteristics. More specifically, when HS S/D was used, increase of defects related with oxygen deficiency such as oxygen vacancy (V_o), ionized oxygen vacancies (Vo^+, Vo^{++}), and interstitial oxygen (O_i) degraded μ_{lin} by impeding carrier transport [14]. In addition, the clockwise-hysteresis shown in Fig. 1(b) is known to be caused by electron trapping in the active layer near the active layer/GI interface [15]. It has been reported that oxygen vacancies can function as shallow trap sites when there is a large open space near them [16], [17]. Therefore, it can be concluded that the TFTs made with the HS S/D showed larger hysteresis due to the increased number of trapped electrons by V_o in the active layer. A similar mechanism has been proposed to explain the degradation of flexible oxide TFTs after the application of bending stress [18]. However, the results of our experiments indicate that the change of intrinsic film stress can affect the electrical performance of oxide TFTs even in the absence of an external stress.

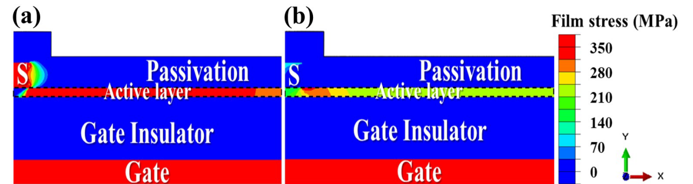

Fig. 4. Stress distribution image of Al-IZTO TFTs using (a) HS S/D, (b) LS S/D (S = Source).

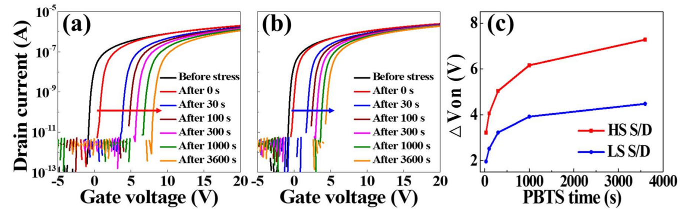

Fig. 5. Transfer curves of Al-IZTO TFTs under PBTS (1 MV/cm, 60 °C) using (a) HS S/D, (b) LS S/D. (c) ΔV_{on} of TFTs as a function of PBTS time.

Fig. 5(a) and (b) present the stabilities of the Al-IZTO TFTs with HS S/D and LS S/D under positive bias temperature stress (PBTS) of 1 MV/cm and 60 °C. After 3600 s under PBTS, the TFT with HS S/D and LS S/D showed V_{on} of 7.28 V and 4.48 V, respectively. Fig. 5(c) shows the V_{on} of TFTs as a function of PBTS time. The positive parallel shift of the transfer curves without degradation of S.S suggests electron trapping as the main cause of the PBTS instability for both cases [19]. Considering the XPS results in Fig. 3, it can be concluded that the TFTs with HS S/D had degraded stability because of more D_o-related electron trapping defects in the active layer [20].

IV. Conclusion

This letter reports the effect of intrinsic film stress of Mo S/D electrodes on the electrical characteristics of Al-IZTO TFTs. Both transfer characteristics and stability of devices were degraded when HS S/D was used. The XPS results and FE simulations suggest that the HS Mo S/D applied sufficient stress in the active layer to break metal-oxygen bonds and generate more D_o-related defects, and consequently deteriorates the overall performance of the Al-IZTO TFTs. We believe that this study provides crucial engineering viewpoint for the future oxide TFT research.

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