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Investigation on the Hump Effect Utilizing the Capacitance–Voltage Characteristics of a-InGaZnO Thin Film Transistor

Dong-Uk Kim[1], Sang-Hee Ko Park[2], Heehwan Choe[1], and Jae-Hong Jeon[1,*]

[1] School of Electronics and Information Engineering, Korea Aerospace University, Goyang 10540, Korea
[2] Department of Materials Science and Engineering, Korea Advanced Institute of Science and Technology, Daejeon 34141, Korea

As well as a parallel shift, the hump effect is also found in the transfer curve of amorphous indium gallium zinc oxide thin film transistors (a-IGZO TFTs) after gate bias stress. The capacitance–voltage (C–V) curve is also deformed from its initial shape after the stress. This study analyzes both the C–V and transfer curves based on the same gate voltage axis to investigate the mechanism driving the hump generation. The origin of the hump effect seems to have little relationship with the electron trapping in the gate insulator. It is deduced that an additional interface trap generation occurs at the a-IGZO interface during gate bias stress test, thereby explaining the origin of the hump effect.

Keywords: Thin Film Transistor, Oxide Semiconductor, Bias Stress, Hump Effect.

1. INTRODUCTION

Recently, oxide semiconductor devices have been utilized as elements in the pixel circuits of commercial flat panel displays. In the future, they will also be used in nano-electronic applications such as sensors and solar cells.[1–4] In particular, amorphous indium gallium zinc oxide thin film transistors (a-IGZO TFTs) have shown high field effect mobility, compatibility with low temperature processes, uniform characteristics, and transparency.[5–8] For commercial utilization, device stability is one of the most important requirements. There have been a lot of studies regarding device stability under various driving conditions.[9–13] A prolonged gate bias is one of the main factors that degrade the electrical characteristics of a device. It is well known that a transfer curve can shift in a lateral direction under positive gate bias in the case of unstable n-channel devices. This is mainly due to the electron trapping that occurs if trap sites exist inside the gate insulator.

In addition to conventional degradation phenomena such as the lateral shift of a transfer curve, the deformation of a transfer curve in the subthreshold region is an anomalous degradation feature. This is known as the hump effect. A few studies have reported that the transfer characteristics of a-IGZO TFTs often reveal a hump shape in the subthreshold regime.[14–16] Some researchers have reported that the hump effect originated from the presence of a parasitic channel acting independently from the main channel.[17, 18]

In the case of our a-IGZO TFT, the hump effect was found after but not before the bias stress test. In order to deduce the mechanism driving the hump generation, the capacitance–voltage (C–V) characteristics as well as the transfer characteristics were investigated. Thus far, little effort has been exerted to analyze the hump effect with C–V characteristics. This may be due to the fact that with the C–V curves, graphical deformation is uncommon. However, the present study found that deformation could be found in devices in which the channel width (W_{ch}) was much larger than the channel length (L_{ch}). From the analysis of the C–V characteristics, the possible mechanism driving the stress-induced hump effect was deduced.

2. EXPERIMENTAL DETAILS

A-IGZO TFTs were fabricated in a top gate structure using conventional photolithography and etching. An indium tin oxide layer was deposited using RF magnetron sputtering,

*Author to whom correspondence should be addressed.

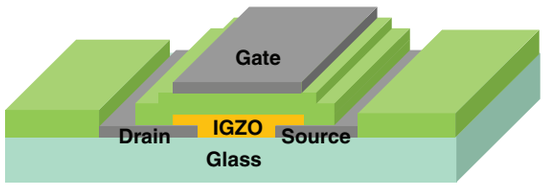

Figure 1. Structure of a-IGZO TFT used in this study.

and it was patterned for the source/drain (*S*/*D*) electrodes. A 40-nm thick a-IGZO active layer was deposited via RF magnetron sputtering at room temperature. The active layer was patterned via a wet etching process. A SiO_2 layer was deposited using plasma enhanced chemical vapor deposition for the gate insulator. A molybdenum gate electrode was deposited via RF magnetron sputtering and patterned with the wet etching method. Finally the device was annealed at 200 °C in a vacuum chamber to optimize its electrical performance. The final device structure is illustrated in Figure 1.

The stress tests were carried out in a shielding box to isolate external light. An Agilent 4155C semiconductor parameter analyzer and a probe positioning system were utilized for the stress tests and the measurement of the transfer characteristics. An Agilent 4284A LCR meter was utilized to measure the *C*–*V* characteristics. For the stress test, a positive gate bias of 20 V was applied to the fabricated TFTs. The source and drain electrodes were connected to a ground (0 V) terminal. The maximum time duration of each stress condition was 10,000 s.

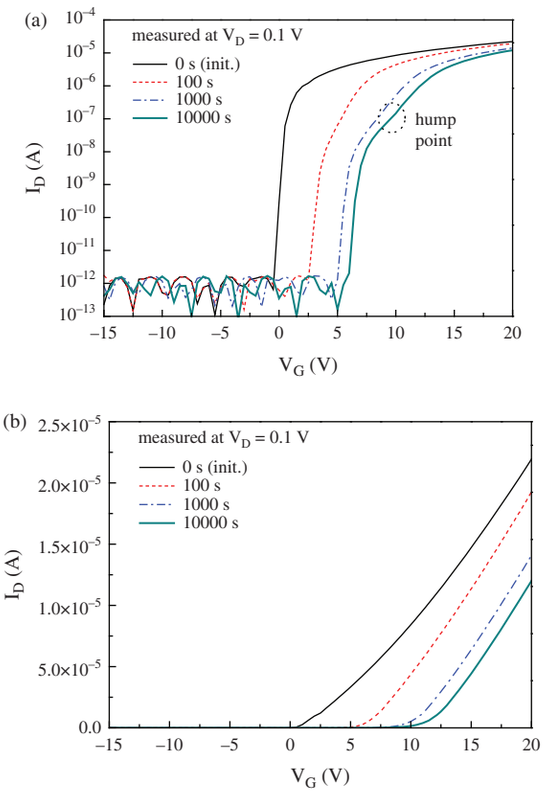

Figure 2. Evolution of changes in the transfer characteristics of a-IGZO TFT during DC 20 V gate bias stress. (a) Log scale plot, (b) linear scale plot.

3. RESULTS AND DISCUSSION

Figure 2 shows the evolution of changes in the transfer characteristics of the a-IGZO TFTs ($W_{ch} = 320\ \mu$m, $L_{ch} = 20\ \mu$m) during the DC 20-V gate bias stress. A considerable lateral shift occurred in the transfer curve. An additional degradation factor caused the curve to seem bumpy in the subthreshold region in the log scale plot. The origins of these degradation phenomena were not easy to deduce by solely relying on the transfer characteristics.

In addition to measuring the transfer characteristics, the *C*–*V* characteristics were also measured before and after the stress. A typical TFT *C*–*V* curve exhibits a stepwise shape composed of the lowest capacitance value on the left side of the curve and the highest value on the right side. The lowest capacitance value originates from the overlap of the gate electrode with the source (or the drain) electrode under negative gate bias far below the threshold voltage (V_{th}). The highest value originates from the overlap of the gate electrode with the source, drain, and channel under positive gate bias far above the V_{th}. The mechanism used to measure the lowest and the highest capacitance can be illustrated using graphical models, as shown in Figure 3.

The *C*–*V* characteristics of our devices were measured with AC small signal of which the amplitude was 0.1 V and the frequency was 0.5 kHz. Figures 4(a) and (b) show the gate-to-source capacitance (C_{GS}) and the gate-to-drain capacitance (C_{GD}), respectively. Each curve was measured while floating one of the source and drain electrodes. C_{GS}, for example, was measured while floating the drain electrode. The initial *C*–*V* curve before the stress produced the conventional stepwise shape. Both the gate-to-source and

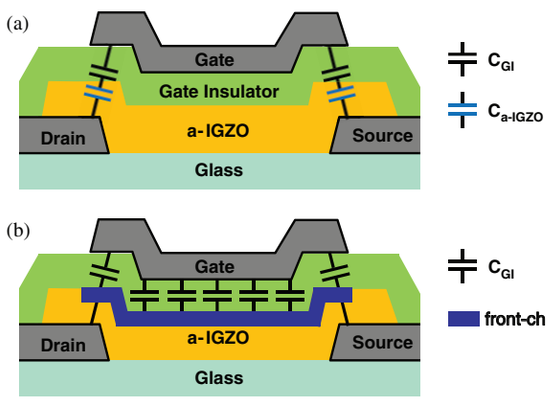

Figure 3. Graphical models illustrating the measurement of the capacitance. (a) The lowest value under negative gate bias far below V_{th}, (b) the highest value under positive gate bias far above V_{th}.

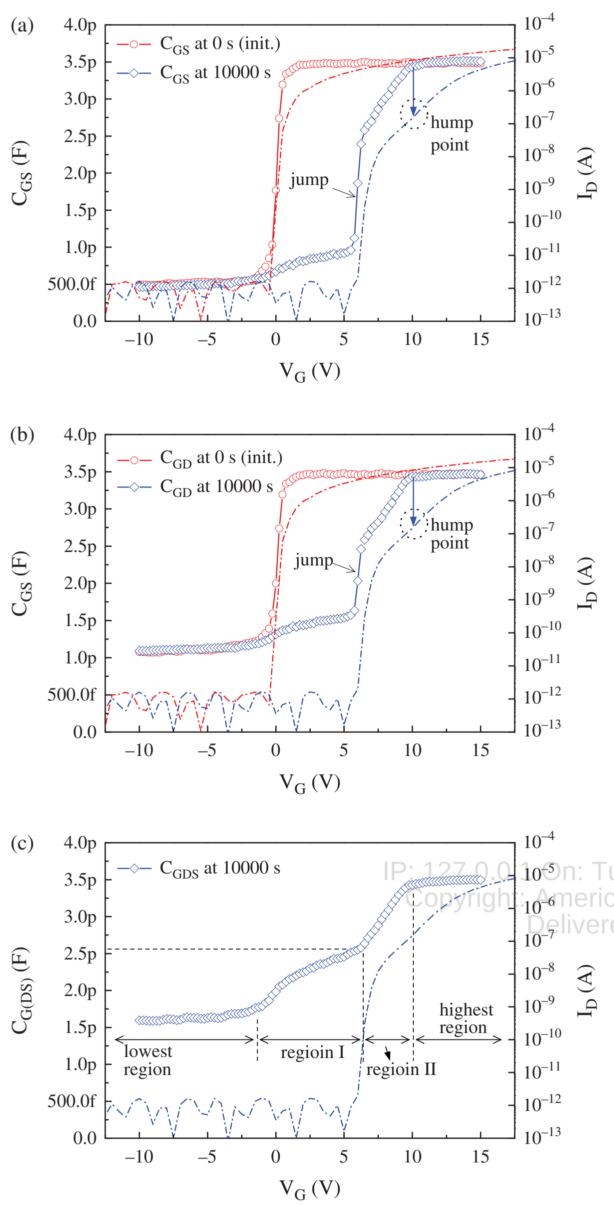

Figure 4. (a) C_{GS} and (b) C_{GD} before and after the gate bias stress ($V_G = 20$ V), (c) $C_{G(DS)}$ after the gate bias stress.

gate-to-drain overlap length were designed to be 10 μm. However, the difference in the lowest capacitance values between C_{GS} and C_{GD} occurred due to the misalignment of a photomask during fabrication.

After the stress, the C–V curve showed considerable deformation from the initial curve with the lateral shift. Crucially, it should be noted that the point at which the highest capacitance started to be measured coincided with the hump point. Generally, in the case of TFTs showing a hump, the overall transfer characteristics are superimposed characteristics of the main and parasitic channels. From the transfer curve, it was deduced that the right side of the hump point represented the characteristics of the main channel and the left side those of the parasitic channel. Therefore, the highest capacitance value for the C–V characteristics started to be measured just after the main channel was induced.

In terms of the graphical deformation, the abrupt jump from the lower to higher value was another interesting feature. This phenomena was found in both the C_{GS} and C_{GD} curves. In order to verify the mechanism driving the distortion, the drain and source electrodes were connected and the capacitance between the gate electrode and connection ($C_{G(DS)}$) was measured. Figure 4(c) shows the C–V curve of the $C_{G(DS)}$ after the stress. In the $C_{G(DS)}$ curve, the abrupt jump, which could be found in either the C_{GS} or C_{GD}, did not appear. The low-to-high transition region was divided into two characteristic regions (Regions I and II). Region I coincided with the sum of the C_{GD} and C_{GS}, and Region II coincided with either the C_{GD} or C_{GS}.

The fact that Region I of the $C_{G(DS)}$ coincides with the sum of the C_{GD} and C_{GS} indicates that Region I belongs to the turn-off mode of the a-IGZO TFT in the transfer curve, so the C_{GD} and C_{GS} are independent of each other. The slight increase in the capacitance value with the gate bias implies that the mechanism of the lateral shift of the transfer curve may not have been related to the electron trapping in the gate insulator. Rather than electron trapping, a greater portion of responsibility for the shift may have stemmed from the interface states. Moreover, it seems likely that the back channel interface was more responsible than the front channel interface because the device exhibited a hump effect related to the parasitic channel. These interface states are considered to have been deep acceptor-like states. Their energy level might be separated from the conduction band edge by more than 1 eV, so the transfer curve measured after the stress shifted along the positive gate voltage axis compared to the curve measured before the stress. The mechanism driving the capacitance increase in Region I with the gate bias is illustrated in a graphical model in Figure 5(a).

The increase in the capacitance value, which appeared as a slope increasing to the highest value in Region II, constitutes another deformation factor in the C–V curve after stress. The low capacitance value at the beginning of Region II was possibly caused by other capacitive components connected in series with the gate insulator capacitance. It is believed that the back channel was activated in Region II. Therefore, the C_{GS} and C_{GD} curves coincided with $C_{G(DS)}$ in Region II. In addition to the generation of deep acceptor-like states during stress, it was probable that cation dangling bonds were generated at the bottom surface. These bonds formed degenerated states, and these states acted as a current path (i.e., the back channel). In this case, the energy level of the degenerate states might be lower than the conduction band edge, so the back channel was induced under the lower gate bias in advance of the formation of the front channel. This is illustrated by the graphical model shown in Figure 5(b). Therefore, the a-IGZO layer acted as another dielectric layer in addition

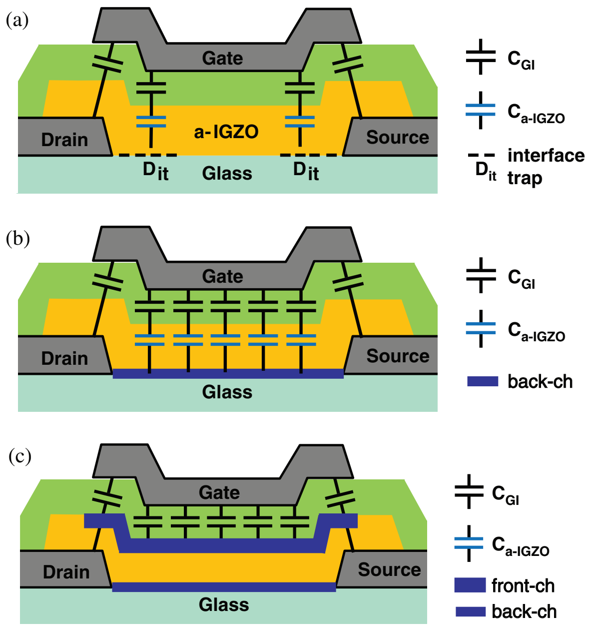

Figure 5. Graphical models illustrating the measurement of the capacitance (a) in the region I, (b) in the region II, (c) at the end of the region II.

to the gate insulator, and the thickness of the whole dielectric layers increased. Therefore, the measured capacitance at the beginning of Region II was lower than the value measured when only the gate insulator acted as a dielectric layer. Furthermore the back channel is generally so resistive that the measured capacitance was able to increase progressively with the gate voltage, which reduced the resistance of the back channel. The total capacitance could be increased with the gate voltage until the front channel was activated at the end of Region II (Fig. 5(c)).

4. CONCLUSION

This study investigated the stress-induced hump effect by analyzing *C–V* characteristics. After the stress, both the *C–V* and transfer curves exhibited considerable deformations in their subthreshold characteristics. In the *C–V* curve, the transitional region appeared on the left side of the hump point and could be divided into two different characteristic regions. It seemed probable that electron trapping was not the origin of the deformation of the *C–V* curve. An additional interface trap generation and the back channel formation at the bottom surface of the a-IGZO was deduced for the origin of the deformation of the *C–V* curve as well as the hump of the transfer curve.

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