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Research Article

Engineering a Subnanometer Interface Tailoring Layer for Precise Hydrogen Incorporation and Defect Passivation for High-End Oxide Thin-Film Transistors

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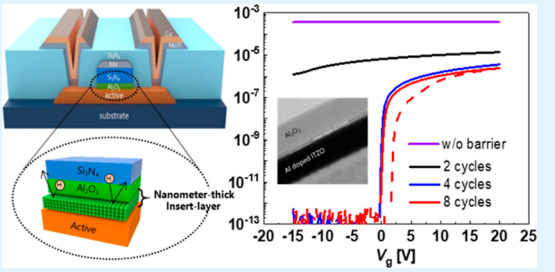
ABSTRACT: Top-gate self-aligned structured oxide thin-film transistors (TFTs) are suitable for the backplanes of high-end displays because of their low parasitic capacitances. The gate insulator (GI) deposition process should be carefully designed to manufacture a highly stable, high-mobility oxide TFT, particularly for a top-gate structure. In this study, a nanometer-thick Al_2O_3 layer via plasma-enhanced atomic layer deposition (PE-ALD) is deposited on the top-gate bottom-contact structured oxide TFT as the interface tailoring layer, which can also act as the hydrogen barrier to modulate carrier generation from hydrogen incorporation into the active layer of the TFT during the following process such as postannealing. Al-doped InSnZnO (Al/ITZO) with an Al/In/Sn/Zn atomic ratio composition of 1.7:24.3:40:34 was used for high mobility oxide semiconductors, and an Al_2O_3/Si_3N_4 bilayer was used for the GI. The degradation issue due to the excellent barrier characteristics of Al_2O_3 and Si_3N_4 can be minimized. An oxide TFT fabricated without the interface tailoring layer exhibits conductor-like characteristics owing to the excessive carrier generation by hydrogen incorporation. However, TFTs with additional interface layers exhibit reasonable characteristics and distinct trends in electrical characteristics depending on the thicknesses of the interface layers. The optimized devices exhibit an average turn-on voltage (V_{on}) of −0.31 V with 33.63 $cm^2/(V\ s)$ of high mobility and 0.09 V/dec of subthreshold swing value. The interfaces between the active layer and hydrogen barriers were investigated using a high-resolution transmission electron microscope, contact angle measurement, and secondary ion mass spectroscopy to reveal the origin of the trends in properties between the devices. The top-gate device with a hydrogen barrier using the four-cycle deposition exhibits optimum electrical characteristics of both high mobility and good stability with only a 0.04 V shift of V_{on} under positive-bias temperature stress (PBTS). We realize a high-end, self-aligned TFT with high mobility [34.7 $cm^2/(V\ s)$] and negligible V_{on} shift of −0.06 V under PBTS by applying a subnanometer hydrogen barrier.



KEYWORDS: *carrier control, defect passivation, stability, high mobility, oxide thin-film transistor (TFT), atomic layer deposition (ALD)*

1. INTRODUCTION

Active-matrix organic and microlight-emitting diodes form the leading next-generation display owing to their vivid color, high efficiency, excellent contrast ratio, flexibility, and lightness.[1−3] They can be suitably applied in high-end, large-area, form-valuable displays. Backplane devices have to be uniform over a large area to drive numerous pixels within a short time for high-resolution and large-area displays. Thin-film transistors (TFTs) with oxide semiconductors satisfy these requirements owing to their outstanding electrical characteristics, process-ability over large areas with good uniformity, and easy fabrication.[4−6]

Several oxide semiconductors, such as indium zinc oxide (IZO),[7] indium oxide (InO),[8] indium tin zinc oxide (ITZO),[9] indium gallium tin oxide (IGTO),[10] and Al-doped ITZO (Al/ITZO),[11] are known to have high mobility. The stoichiometry of oxide semiconductors is crucial in electrical characterization,[12] and the mobility of oxide semiconductors can be further improved by optimizing the composition.[13] These oxide semiconductors are easily and uniformly deposited by sputtering for high-end display backplanes. Among various oxide TFT structures, a self-aligned structure offers the advantage of reduced resistance−capacitance delay that is generated by the parasitic capacitance between the gate and source/drain, irrespective of the gate insulator (GI).[14−16] Additionally, a high on-current can be obtained with a self-aligned structure using a GI of high-k materials, such as HfO_2[17] and Y_2O_3.[18] Furthermore, to prevent the thermionic emission of electrons and holes from the oxide semiconductor to the insulator owing to the low band offset and Al_2O_3,[19] multilayers,

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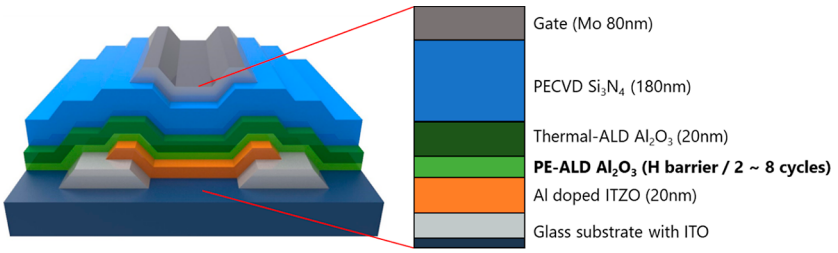

Figure 1. Schematic of a high-mobility TFT with an ultrathin hydrogen barrier layer.

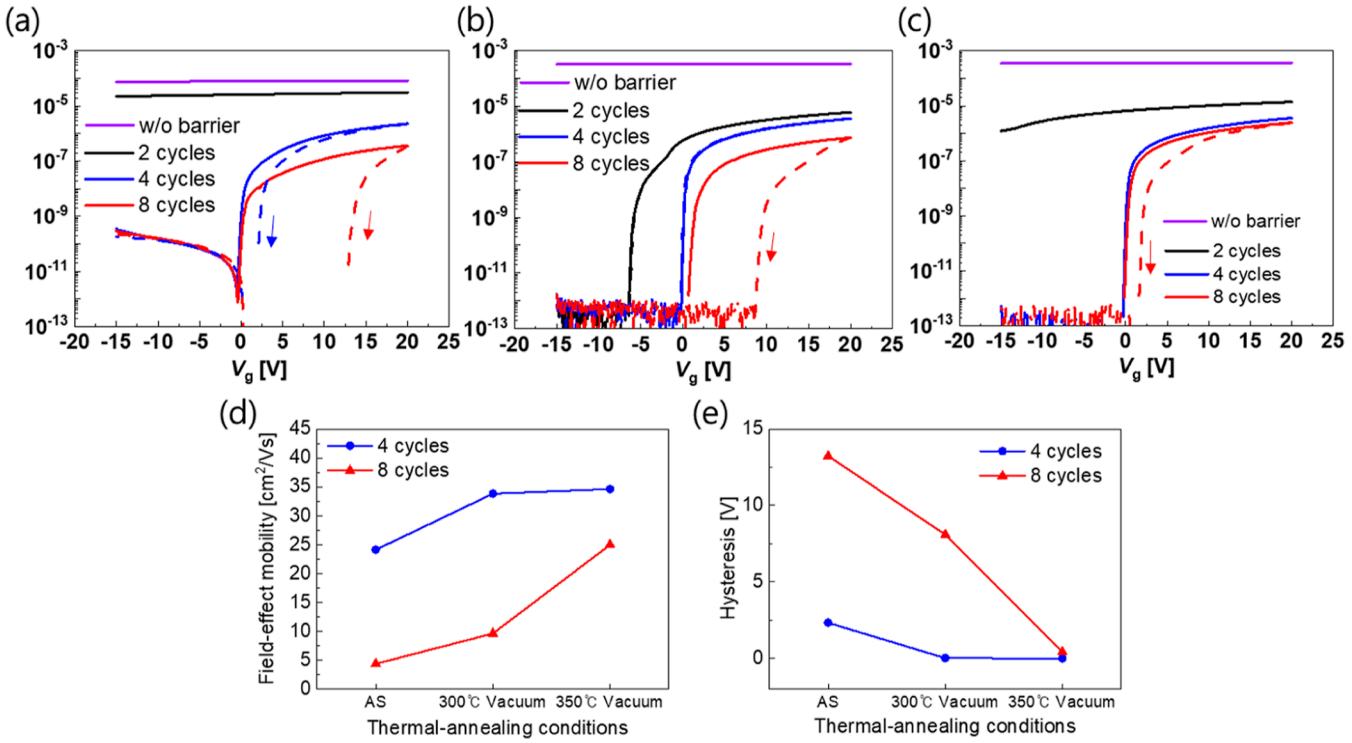

Figure 2. Transfer characteristics of TFTs with different thicknesses of barrier conditions: (a) before annealing, (b) after vacuum annealing at 330 °C, and (c) after vacuum annealing at 350 °C. The trends of (d) field-effect mobility and (e) hysteresis are based on the thermal annealing temperature.

such as Al_2O_3/Si_3N_4[3,20] bilayers, or multicomponent doping have been investigated.[21] However, realizing reasonable electrical characteristics of high-mobility oxide TFTs with a top-gate structure is challenging. Because a GI is deposited on an oxide semiconductor in the top-gate structure, the doping effect of hydrogen during GI deposition and subsequent processes, including postannealing, cannot be avoided. In particular, the GI deposition process must be carefully designed in terms of hydrogen incorporation, while fabricating oxide TFTs with high mobility and stability. Although this phenomenon renders the yield of normal transfer characteristics in high-mobility oxide TFT complex owing to the creation of excessive carriers,[22−24] it passivates traps to improve the electrical reliability of the TFTs.[25,26] Therefore, hydrogen incorporation must be appropriately controlled. Studies to improve the electrical characteristics of oxide TFTs by incorporating hydrogen through gas annealing[27] or plasma treatment are underway.[26,28] However, novel methodologies to precisely control the incorporation of hydrogen are required because the V_{on} characteristic is very sensitive to the amounts of hydrogen in high-mobility oxide TFTs. In this study, ultrathin additional layers were applied between the active layer and GI as the novel methodology for the precise control of hydrogen incorporation.

We fabricate high-end, top-gate-structured oxide TFTs with an Al_2O_3/Si_3N_4 bilayered GI.[3,20] We modulate the amount of hydrogen diffused from the SiN_x into the active layer by utilizing Al_2O_3, which is deposited using a combination of plasma-enhanced atomic layer deposition (PE-ALD) and thermal ALD. An ALD process can be classified into thermal and PE-ALD, which use H_2O as the oxidant and O_2 plasma, respectively. Thermal ALD causes a large amount of hydrogen incorporation owing to the H_2O oxidant. Based on a preliminary study, the use of thermal-ALD-processed Al_2O_3 film as the GI of oxide TFT degraded the transfer characteristics of oxide TFTs because of hydrogen incorporation.[3] In this study, an ultrathin layer of Al_2O_3 is deposited by PE-ALD as a hydrogen barrier before further deposition by thermal-ALD resulting in hydrogen incorporation. The electrical characteristics of the fabricated TFTs are investigated relative to the interface layer deposited by PE-ALD. We performed high-resolution transmission electron microscopy (HRTEM), contact angle measurements, and secondary ion mass spectroscopy (SIMS) to validate the differences in the

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electrical characteristics of the TFTs and the effects of the hydrogen barrier. We achieve high-mobility oxide TFTs with stable characteristics by controlling hydrogen incorporation through the deposition of a nanometer-thick barrier layer by PE-ALD.

2. EXPERIMENTAL SECTION

Top-gate bottom-contact TFTs were fabricated under different GI deposition conditions. Because top-gate bottom-contact TFTs have the same stacking sequence of active layers and GIs as those of self-aligned TFTs, they are suitable for investigating the effects of GIs and their deposition processes on the electrical characteristics of oxide TFTs. Each layer was aligned using photolithography with a photo mask for the fabrication of the devices.

Indium tin oxide was patterned as the source and drain, and 20 nm of Al/ITZO, which is an actively researched high-mobility oxide semiconductor,[11] was deposited via sputtering. The comparison of the electrical characteristics of the Al/ITZO and other researched oxide semiconductors is listed in Table S1.[3,8,11,13,29−31] While Al/ITZO did not reach the high-mobility characteristics of ALD-processed a-IGZO with optimized composition,[13] it exhibited mobility of approximately 30 $cm^2/(V\ s)$, similar to well-known high-mobility oxide semiconductors, such as IZO, InOx, and ITZO. Furthermore, Al/ITZO demonstrates good endurance against chemicals, such as photoresist (PR) and PR stripper.[11] Therefore, the effects of the GI process should be investigated preferably by excluding the side effects of chemical damage. A stack of 20 and 180 nm Al_2O_3 and Si_3N_4, respectively, was adopted as the GI because these structures have been reported as attractive GIs for high-end devices.[3,20] At 200 °C, the Al_2O_3 layer was deposited via thermal-ALD with a trimethylaluminum precursor as the Al source, whereas the Si_3N_4 layer was deposited by plasma-enhanced chemical vapor deposition (PE-CVD). To mitigate the incorporation of hydrogen, an ultrathin Al_2O_3 layer was deposited via PE-ALD as a hydrogen barrier prior to GI deposition. The electrical characteristics of the devices were investigated based on the number of deposition cycles of the hydrogen barrier, with two, four, and eight cycles of PE-ALD. Growth per cycle (GPC) was used to calculate the hydrogen barrier thicknesses as 0.25, 0.5, and 1.0 nm, respectively. Finally, Mo, a widely used electrode material, was deposited and patterned as the gate electrode.[32] A schematic of the fabricated oxide TFT is shown in Figure 1. The fabricated TFTs were annealed at 330 and 350 °C under vacuum conditions. The electrical and stability characteristics of the devices were investigated in dark conditions to exclude the light radiation effect using the Agilent 4284A precision LCR meter and B4156A semiconductor parameter analyzer with a probe station.[33,34] The interfaces between the active layer and GIs were scrutinized with HRTEM, contact angle measurements, and SIMS to investigate the origin of the differences in the electrical characteristics of the TFTs.

3. RESULTS AND DISCUSSION

The fabricated devices showed distinct trends in electrical characteristics depending on the thickness of the hydrogen barrier. The transfer characteristics and electrical parameters of each TFT based on the thermal annealing conditions are shown in Figure 2. (12 overlapped transfer characteristics in the linear and saturation regions for each sample after thermal annealing at 350 °C are shown in Figure S1 in the Supporting Information). A drain voltage (V_d) of 0.1 V was applied to the TFT with a length and width of 40 and 20 μm, respectively. The solid and dashed lines on the graph represent the forward and reverse sweeps, respectively. The oxide TFT without the hydrogen barrier struggled to exhibit normal ON/OFF characteristics owing to excessive hydrogen incorporation from the following processes, as shown in Figure 2. Additionally, the oxide TFT with two cycles of hydrogen barrier showed conductive or negatively shifted characteristics, indicating the insufficiency of the two cycles of PE-ALD-deposited Al_2O_3 to prevent hydrogen incorporation from processes, such as GI deposition and postannealing. In addition, the device with two cycles of barrier exhibited conductor-like behavior in as state. Sputtered oxide semiconductors require a further activation process through thermal annealing to stabilize the channel against the generated scattering center, ionized oxygen vacancies (V_o^+), and weak oxygen bonding.[35] Furthermore, in the top-gate structure, the GI and gate metal deposited on top of the active layer expose the oxide semiconductor to UV irradiation during plasma of the CVD process and sputtering for the GI and gate metal deposition, respectively. This UV exposure results in carrier generation and facilitates the formation of the conductive channel.[30,33] After thermal annealing at 330 °C, the devices exhibited ON/OFF characteristics owing to the activation of the oxide semiconductor by thermal energy, restoration of generated free carriers by UV, and curing of donor-like defects, such as V_o and weakly bonded O−H.[36,37] Further annealing at a higher temperature of 350 °C resulted in more hydrogen diffusion into the oxide semiconductor and generated free carriers, resulting in conductive behavior. The devices with four and eight cycles of the hydrogen barrier process exhibited ON/OFF characteristics prior to thermal annealing owing to the thicker barrier compared to those of two cycles. This resulted in a reduced hydrogen incorporation. In addition, the high OFF current indicates that sputtered oxide semiconductors required an additional activation process with thermal energy, as earlier mentioned. After thermal annealing, the devices showed reasonable transfer characteristics. Particularly, the oxide TFT with four hydrogen barrier cycles exhibited exceptional transfer characteristics, whereas that with eight hydrogen barrier cycles exhibited hysteresis-like characteristics. The devices exhibit increased conductivity as the annealing temperature increased from 330 to 350 °C. Thermal annealing induces hydrogen diffusion from the GI to the active layer, which can be enhanced at a higher temperature because hydrogen diffusivity generally increases with temperature.[38] In general, hydrogen increases carrier density in oxide semiconductors by acting as a shallow donor.[22−24] Consequently, the conductivity of the devices is increased, owing to the increase in free carriers.

The results of the extracted electrical parameters obtained based on thermal annealing are shown in Figure 2d,e. The value of μ_{FE} was calculated as follows

$$\mu_{FE} = \frac{g_m}{\frac{W}{L} \times C_i \times V_d} \quad \left(\text{where } g_m \equiv \frac{\partial I_d}{\partial V_g}\right) \tag{1}$$

where W and L denote the channel width and length, respectively, and C_i is the capacitance of the GI; the measured value of the double-layered GI was approximately 3.1 pF/m^2. The electrical properties of the devices improved with an increase in the thermal annealing temperature because hydrogen diffusion increased from the thermal-ALD Al_2O_3 layer, through the hydrogen barrier (deposited by PE-ALD), into the oxide semiconductor, resulting in the passivation of more defects. The PE-ALD process utilized for the hydrogen barrier can induce plasma damage and generate shallow defects, resulting in clockwise hysteresis. However, these defects can be effectively passivated by hydrogen incorporation.[39] A thicker hydrogen barrier could result in a larger number of defects remaining unpassivated by inhibiting

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hydrogen diffusion into the oxide semiconductor. In addition, more shallow defects are generated owing to the employment of more hydrogen barrier cycles. Consequently, the device with eight hydrogen barrier cycles exhibits a relatively large hysteresis with a value of 0.49 V. The extracted average values of electrical parameters for 12 devices are listed in Table 1. The devices with four hydrogen barrier cycles exhibit optimized electrical characteristics with a high mobility of 33.63 $cm^2/(V\ s)$ and negligible hysteresis.

Table 1. Extracted Electrical Parameters with Average and Standard Deviation for 12 Devices with Different Barrier Thicknesses after Vacuum Annealing at 350 °C

cycles of barriers [cy]	V_{on} [V]	μ_{lin} [$cm^2/(V\ s)$]	SS [V/dec]	hysteresis [V]
2	NA	NA	NA	NA
4	−0.31 ± 0.16	33.63 ± 0.82	0.09 ± 0.01	0.035 ± 0.03
8	−0.08 ± 0.30	22.61 ± 1.09	0.12 ± 0.01	1.579 ± 0.55

The hydrogen barriers deposited for this study were thin with thicknesses of less than 1.0 nm. The thin hydrogen barriers were expected to physically block hydrogen and hinder carrier generation through other factors. HRTEM images of cross-sectional oxide semiconductor/Al_2O_3 stacks were analyzed to investigate the interfaces between the oxide semiconductor and Al_2O_3 layer, as shown in Figure 3. While the

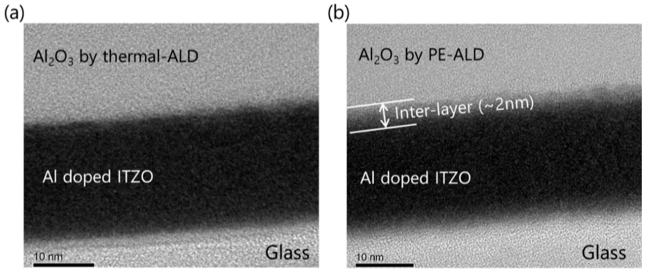

Figure 3. HRTEM images of cross-sectional film stacks with Al_2O_3 deposited by (a) thermal-ALD and (b) PE-ALD.

TEM image showed a clear interface between the thermal-ALD Al_2O_3 layer and oxide semiconductor, an interlayer was observed in the film deposited using PE-ALD. The interlayer reportedly contained defects, including dangling bonds, which resulted in the utilization of incorporated hydrogen to passivate these defects.[40,41] Furthermore, cross-sectional images were acquired based on the number of cycles of the hydrogen barrier, and the interlayer structure was clearly observed after a few cycles of hydrogen barrier deposition, as shown in Figure S2.

The defective interlayer formation was confirmed by the decrease in the contact angle measured after a few cycles of the Al_2O_3 layer via PE-ALD, as shown in Figure 4. The pristine oxide semiconductor had a contact angle of 99.8°, as shown in the inset of Figure 4a. However, after PE-ALD for Al_2O_3, the contact angle decreased considerably to less than 15°, whereas a large contact angle was maintained when Al_2O_3 was deposited via thermal ALD. This defect-induced hydrophilic behavior owing to dangling bonds resulted in a small contact angle,[42] thus reducing hydrogen diffusion through the very thin Al_2O_3 layer deposited via PE-ALD and the defective interlayer.

The depth profiles of hydrogen and OH in film samples with the same stack sequence as the fabricated top-gate structured device were investigated by using SIMS, as shown in Figure 5a,b, respectively. The incorporation of hydrogen and OH in the oxide semiconductor decreased with the application of additional hydrogen barriers, meaning the use of a subnanometer thick hydrogen barrier effectively reduced the diffusion of hydrogen into the oxide semiconductor, leading to devices with reasonable transfer characteristics and moderate carrier concentrations. Although only a minor difference in the OH concentration between the samples was observed, the device with two cycles of the hydrogen barrier process showed conductor-like characteristics, whereas those with four and eight hydrogen-barrier cycles exhibited transfer characteristics. The significant difference in electrical characteristics was attributed to the large number of intrinsic carriers in high-mobility oxide semiconductors. The degradation of the ON/OFF characteristics owing to extra carrier generation was more sensitive in high-mobility cases.[43] Hence, even in small amounts, hydrogen diffusion must be finely controlled, particularly in high-mobility oxide TFTs. Thus, the adoption of a hydrogen barrier produced by ALD is an appropriate process, owing to its controllable atomic thickness. In fact, no significant difference was observed in the composition of hydrogen based on the cycles of barriers. However, smaller amounts of OH were detected in the oxide semiconductor when thicker barriers were applied. Based on previous studies, hydrogen can exist in various forms within oxide semiconductors, including hydrogen interstitial bonding with oxygen (H_i^+), bonding with metal (H_i^-), combined with V_o (H_o^+), and complex of $V_o^0 + H_i^-$ (H-DX$^-$).[44,45] Therefore, the hydrogen in oxide semiconductors can exist in various forms,

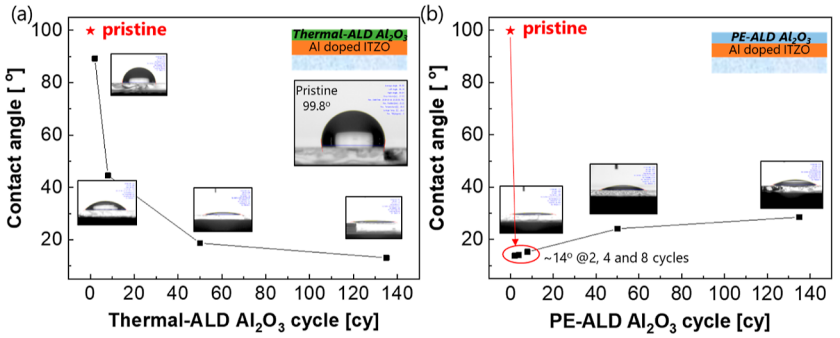

Figure 4. Contact angle variation on the oxide semiconductor surface with cycles of (a) thermal-ALD and (b) PE-ALD for Al_2O_3 layer deposition. The inset indicates the contact angle of the pristine oxide semiconductor.

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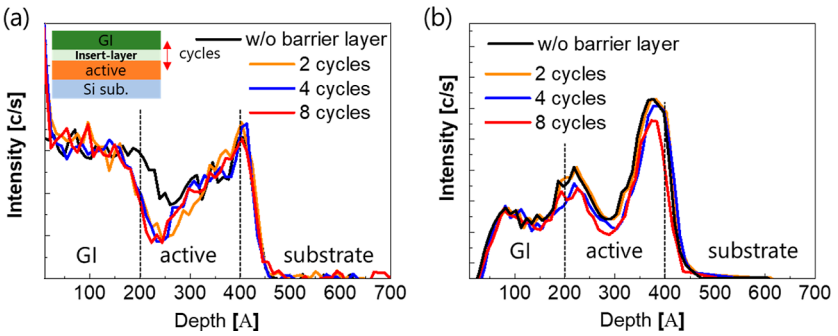

Figure 5. Depth profiles of (a) H and (b) OH in the GI/active/substrate structure with different H barrier thicknesses.

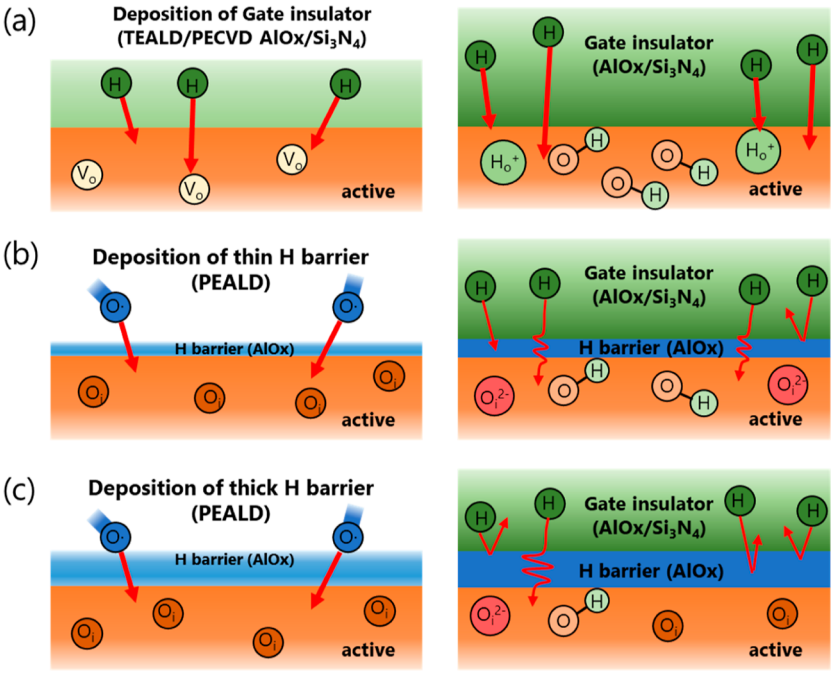

Figure 6. Illustration of a possible hydrogen incorporation mechanism in the case of (a) without an additional barrier and (b) with thin and (c) thick hydrogen barrier deposition processes.

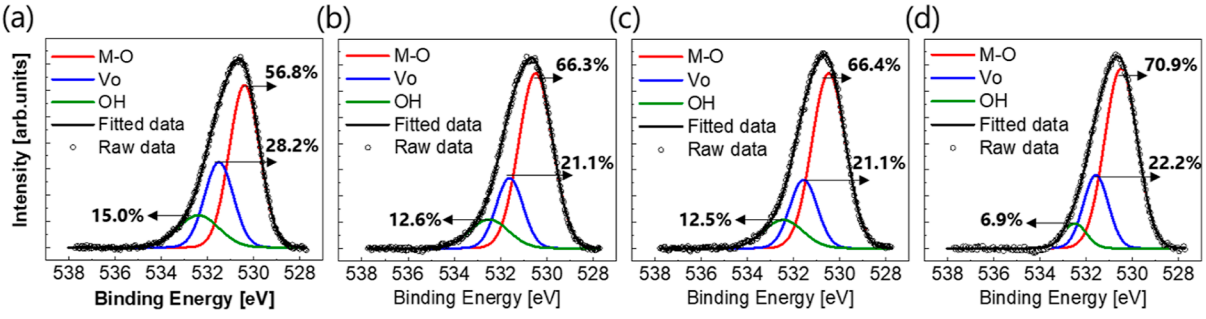

Figure 7. Spectra of XPS O 1s for the active layer surface (a) without additional barrier, (b) with two cycles, (c) four cycles, and (d) eight cycles of the barrier.

including both hydrogen and OH. However, distinguishing the different bonding forms of the hydrogen analyzed by SIMS is challenging because the high-energy secondary ions used in the measurement can break the bonding of the elements. However, the bonding between O−H is quite strong compared with the hydrogen in V_o sites, indicating that much of the hydrogen detected by SIMS is likely combined with V_o and the hydrogen bonding with oxygen is detected in the form of OH.[44] As shown in Figure 6a, without additional barriers, hydrogens can be easily introduced into the oxide semiconductor and placed in V_o sites or bonded with oxygen. Therefore, a relatively large amount of both hydrogen and OH was detected in the SIMS depth profile. In contrast, when additional barriers were applied, the negligible difference in the hydrogen depth profile suggested that the V_o state on the active surface remained the same regardless of the cycles of the hydrogen barrier. This is

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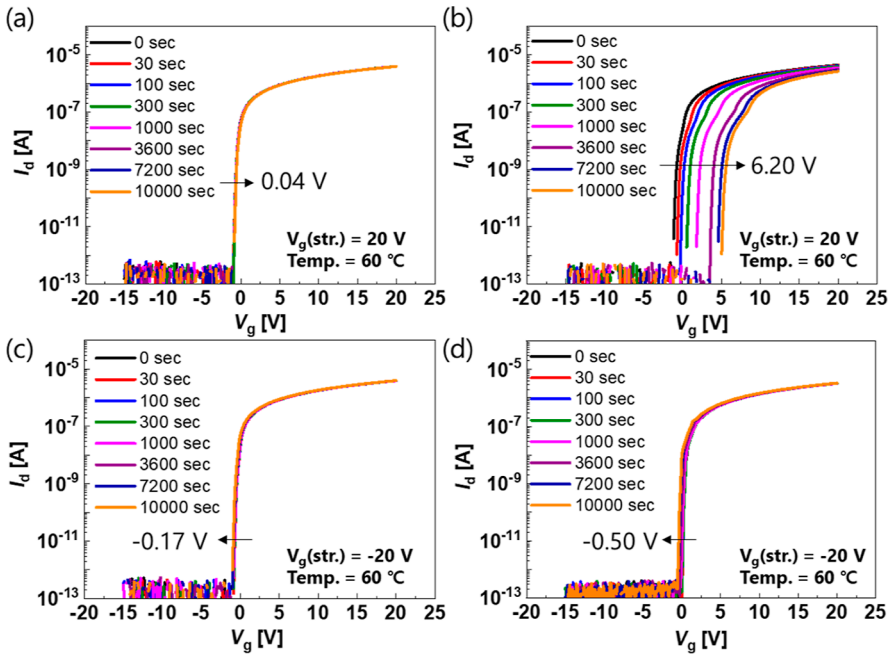

Figure 8. Evaluation of device transfer curves with (a,c) four and (b,d) eight hydrogen barrier cycles under PBTS ($V_{g,str}$ = 20 V, Temp. = 60 °C) and NBTS ($V_{g,str}$ = −20 V, Temp. = 60 °C).

because even a few cycles of the PE-ALD process could inject sufficient oxygen into the underlying oxide semiconductors during oxygen plasma, reducing the V_o states as shown in Figure 6b,c. Consequently, the differences in the degree of hydrogen incorporation were primarily observed in the OH depth profile rather than in the hydrogen depth profile. Although hydrogen and OH rapidly increased at the substrate interface owing to the interface effect in SIMS, it is clearly observed that the hydrogen incorporation tends to decrease as the thickness of the barrier increases.[46]

X-ray photoelectron spectroscopy (XPS) analysis was conducted to validate the effect of hydrogen barrier deposition on the oxygen bonding state in the oxide semiconductors. We scrutinize the O 1s peaks of the film samples with the same stack sequence as the fabricated top-gate structured device, according to the hydrogen barrier cycles at the surface region of oxide semiconductors. The O 1s peaks were deconvoluted into the metal−oxygen bonding (M−O), V_o, and OH centered at 530.4 ± 0.1, 531.5 ± 0.1, and 532.5 ± 0.1 eV, respectively, as shown in Figure 7.[35,47] The portion of V_o decreased from 28.2% to approximately 21% when hydrogen barriers applied. Notably, the deposition process of two cycles of hydrogen barrier effectively reduced V_o, and it barely changed with increasing cycles of hydrogen barriers. Therefore, a similar hydrogen depth profile was observed in the SIMS results, owing to the negligible difference in V_o sites within the oxide semiconductor according to the thickness of the hydrogen barrier. The difference in the degree of incorporated hydrogens according to the thickness of the hydrogen barrier was observed in OH depth profiles, which was also validated in the XPS results. The portion of OH in the O 1s peaks decreased from 12.5 to 6.9% as the cycles of hydrogen barriers increased from two to eight cycles. In summary, an increase in the cycle of the hydrogen barrier decreased the total amount of hydrogen introduced to oxide semiconductors.

The transfer characteristics and stability of high-mobility oxide TFTs were significantly influenced by the thickness of the hydrogen barrier. The overlapped transfer curves obtained under positive-bias temperature stress (PBTS) and negative-bias temperature stress (NBTS) conditions are shown in Figure 8. The transfer characteristics of the oxide TFTs with four hydrogen barrier cycles barely changed under PBTS, whereas the transfer curve shifted significantly in the positive direction when a thicker hydrogen barrier of eight cycles was used, as shown in Figure 8a,b. The time dependence of V_{on} under PBTS and stretched exponential fitting is shown in Figure S3. The device with four hydrogen barrier cycles exhibited a 0.05 V shift in V_{on} after 10 000 s under PBTS, whereas after days, a shift of 0.18 V was expected under PBTS, extracted by the stretched exponential fitting. The difference in the electrical reliability of the devices resulted from variations in hydrogen and the excess oxygen incorporation into the active layer. Numerous studies explored the role of hydrogen as a defect passivator and improvements in electrical stability.[25,26] According to the studies, hydrogen passivates electron-trap sites by bonding with structural defects, such as dangling bonds, or acceptor-like traps, such as oxygen interstitials (O_i). From the possible mechanism in Figure 6b,c, during the deposition of hydrogen barriers, excess oxygen can be introduced to oxide semiconductors owing to oxygen plasma, as validated by results of the comparison in the XPS O 1s peaks. When an optimized thickness of the hydrogen barrier was adopted (four cycles), a moderate amount of hydrogen was incorporated, which passivated the defect states by ionizing the O_i or bonding with dangling bonds.[45,48] The ionized O_i could not trap further free electrons, resulting in the TFT with four cycles of the barrier exhibiting good PBTS stability. In contrast, when a thicker hydrogen barrier was applied, fewer hydrogens were introduced, and more structural or acceptor-like defects remained unpassivated, as shown in Figure 6c. Therefore, the device with eight cycles of barrier exhibited degraded stability under PBTS. In addition, the device with eight hydrogen barrier cycles exhibited hump generation during the PBTS, indicating that the additional

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creation of new acceptor-like states and induced oxygen was crucial in V_{th} instability and the hump characteristics.[49] The varying stability results were attributable to the modulation of hydrogen, achieved through the use of an atomically thick hydrogen barrier, which effectively passivated trap sites while maintaining the ON/OFF characteristics of the TFT. In the case of NBTS stability, both devices with four and eight hydrogen barrier cycles exhibited a small change in V_{on}, as shown in Figure 8c,d, attributed to fewer holes compared with electrons in n-type oxide semiconductors.[50] However, V_o acted as a hole trap center and induced a negative shift during NBTS.[51] From the previous XPS results, the V_o sites were effectively reduced during hydrogen barrier deposition through the oxygen plasma. Consequently, both devices with four and eight hydrogen barrier cycles barely showed changes in V_{on} under NBTS.

Furthermore, we investigated the decrease in drain current during on-state bias, which resulted in variations in the brightness of the current-driven displays. To measure the normalized change in drain current, we applied biases of V_d = 5.5 V and V_g = 5 V, which corresponded to the saturation region (the output characteristics of the measured devices are shown in Figure S5). The results in Figure 9 showed a decrease

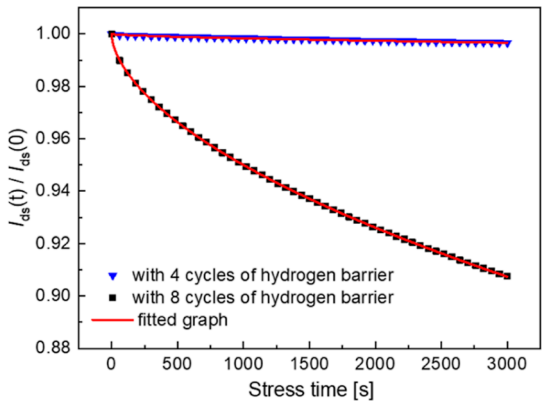

Figure 9. Decay of the normalized drain current during bias stress and fitted curves with stretched exponential formulas.

in drain current under an on-bias condition owing to the screening of the gate bias by the trapped charges. The on-current decay was modeled using a stretched exponential equation, as follows

$$\frac{I_D(t)}{I_D(0)} = \exp\left[-\left(\frac{t}{\tau}\right)^{\beta}\right] \quad (2)$$

where $I_D(0)$ denotes the initial state of the drain current (t = 0), β is the dispersion parameter related to the trap distribution, and τ is the characteristic time for carrier trapping. The red lines in Figure 9 represent the fitting results obtained from eq 2. The results were in good agreement with our experimental results. Thus, current decay measurements supported the stretched exponential model, indicating the dominant cause of these instabilities as charge trapping at the defect sites.[52−54] The values of τ and β were extracted from the fitted curve and are listed in Table 2. The TFT with eight cycles of the thick hydrogen barrier had a considerably higher value of τ compared to that of the TFT with four hydrogen barrier cycles. Therefore, TFT with four hydrogen barrier cycles had significantly fewer trap sites.

Table 2. Extracted Characteristic Time for Trapping (τ) and Dispersion Parameters from the Current Decay Results

cycles of barriers [cy]	τ [s]	β
4	2.2×10^8	0.64
8	1.5×10^5	0.57

Intrinsic subgap states near the conduction band of each device were investigated using the differential ideality factor technique (DIFT),[55] as shown in Figure 10. The subgap states were extracted and decomposed into relatively deep and tail states as follows

$$g_A(E) = N_{TA} \exp\left(\frac{E - E_C}{kT_{TA}}\right) + N_{DA} \exp\left(\frac{E - E_C}{kT_{DA}}\right) \quad (3)$$

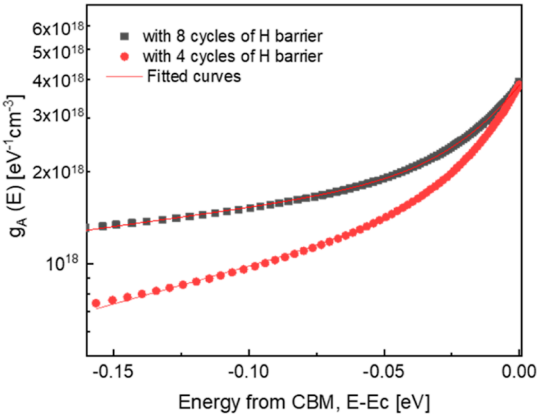

Figure 10. Subgap states of the devices derived using the DIFT based on the hydrogen barrier conditions.

The fitted results are indicated by red lines in Figure 10, whereas the parameters extracted according to the hydrogen barrier conditions are listed in Table 3. Based on the graph and

Table 3. Comparison of Extracted Sub-Gap States Parameters According to the Hydrogen Barrier Conditions

cycles of barriers [cy]	N_{TA} [cm^{-3} eV^{-1}]	kT_{TA} [eV]	N_{DA} [cm^{-3} eV^{-1}]	kT_{DA} [eV]
4	2.10×10^{18}	0.02	1.71×10^{18}	0.18
8	2.09×10^{18}	0.02	1.94×10^{18}	0.41

extracted parameters, the device with a hydrogen barrier formed by four-cycles PE-ALD had a lower subgap state, particularly in the deep state, which was passivated with hydrogen.[56] Therefore, a relatively higher amount of hydrogen was incorporated into the oxide semiconductor when four hydrogen barrier cycles were applied compared with eight cycles, resulting in a more effective defect passivation. Consequently, the device exhibited highly stable electrical characteristics.

Finally, we fabricated a self-aligned oxide TFT, as shown in Figure 11a. To achieve highly stable high-mobility performance, the hydrogen barrier formed by four cycles of the Al_2O_3 layer via PE-ALD was adopted as the optimal condition and validated in top-gate bottom-contact structured devices. The transfer characteristics for the self-aligned oxide TFT with an optimized hydrogen barrier are shown in Figure 11b, and its electrical parameters are listed in Table 4. The results of the

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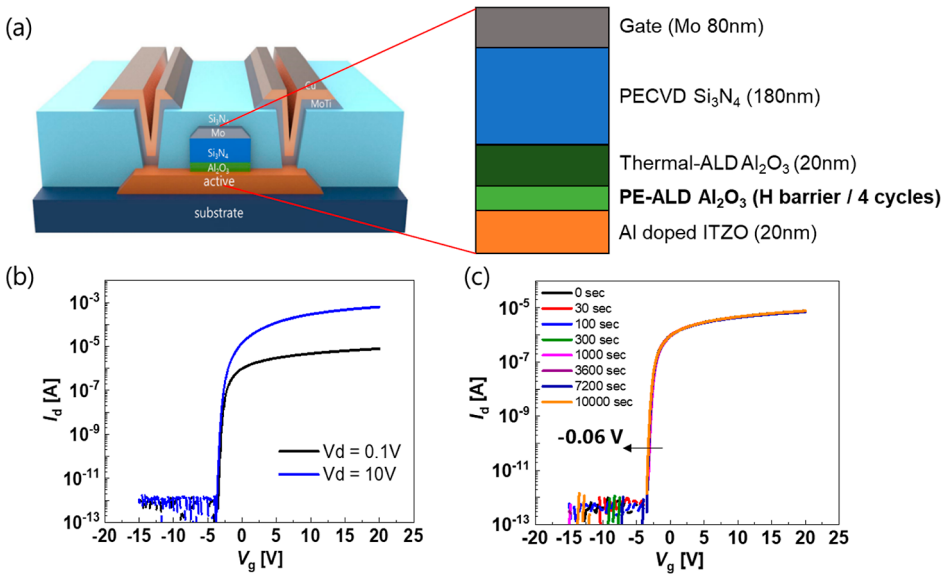

Figure 11. (a) Schematic of the self-aligned TFT with a hydrogen barrier. (b) Transfer curve of the self-aligned TFT with four hydrogen barrier cycles. (c) Overlapped transfer curve under PBTS of over 10 000 s.

Table 4. Electrical Parameters of the Self-Aligned TFT with Four Hydrogen Barrier Cycles

SS (V/dec)	V_{on} [V]	hysteresis [V]	μ_{lin} [$cm^2/(V\ s)$]
0.13 ± 0.003	−3.5 ± 0.29	0.014 ± 0.04	34.7 ± 1.25

transfer curves of 10 devices overlapped for validation of the reproducibility, as shown in Figure S5. The device exhibited high mobility characteristics of 34.7 $cm^2/(V\ s)$; however, the $I-V$ curve was slightly shifted in the negative direction. This negative shift was caused by a decrease in the effective channel length owing to the incorporation of hydrogen during the deposition of the interdielectric layer of SiN_x.[57] The self-aligned oxide TFT demonstrated outstanding stability under PBTS, as shown in Figure 11c, which could be compared with that of a previously evaluated top-gate bottom-contact-structured device. The device also exhibited negligible changes under NBTS owing to fewer defects and holes, as shown in Figure S6. While the top-gate bottom-contact device exhibited normal behavior, the self-aligned oxide TFT showed abnormalities with a slight negative-direction shift in V_{on} during PBTS. This phenomenon could not be explained by electron trapping during PBTS and was believed to have resulted from other factors. The occurrence of abnormal negative shifts under PBTS owing to the H^+ incorporation into the active layer under PBTS has been investigated.[58,59] In self-aligned structures, more hydrogen was incorporated by lateral diffusion from the interlayer dielectric than that in top-gate bottom-contact structures. This was validated by the V_{on} characteristics of the initial transfer curve. The top-gate structured device with two hydrogen barrier cycles, with significant hydrogen incorporation, showed results similar to those of the self-aligned structured device. It exhibited a negative shift in V_{on} under PBTS, indicating significant hydrogen incorporation. The device with two cycles of the barrier exhibited a negative shift in V_{on} under PBTS conditions, similar to the self-aligned structure with comparable initial V_{on} characteristics, as shown in Figure S7. Therefore, the abnormal shift observed under PBTS in the self-aligned device can be attributed to H^+ incorporation, and it can be improved by optimizing metallization or metal contact.[60,61]

4. CONCLUSIONS

We developed highly stable, high-mobility oxide TFTs by adopting subnanometer PEALD-deposited Al_2O_3 as an interface-tailoring layer to modulate hydrogen incorporation into the channel and defect passivation. A nanometer-thick Al_2O_3 layer was deposited by a few cycles of PE-ALD and applied as a hydrogen barrier prior to thermal ALD. Oxide TFT without hydrogen barriers struggled to exhibit normal transfer characteristics because of the large amount of incorporated hydrogen. However, devices with additional interface layers exhibited reasonable transfer characteristics. Structural and interface investigations through TEM and contact angle measurements revealed that the formation of defective regions during PE-ALD effectively prevented carrier generation caused by hydrogen incorporation. The electrical characteristics of the devices varied significantly depending on the thickness of the hydrogen barrier. Based on SIMS depth profiles, hydrogen diffusion into the active layer differed depending on the barrier thickness, and O 1s peaks in XPS results indicated that barrier deposition modified the bonding state of oxide semiconductors. When the hydrogen barrier layer deposited by four cycles of the PE-ALD process was adopted, high mobility and high stability characteristics were obtained. Finally, the high-end self-aligned oxide TFT, fabricated with four hydrogen barrier cycles, exhibited a high mobility of 34.7 $cm^2/(V\ s)$, whereas V_{on} barely shifted under PBTS over 10 000 s at 60 °C.

■ ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acsami.3c10185.

Overlapped transfer curves of 12 samples after thermal annealing at 350 °C; HRTEM images of cross-sectional film stacks of the oxide semiconductor and Al_2O_3 layer according to the hydrogen barrier condition; time dependence of V_{on} under the PBTS condition for

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devices with four and eight cycles of hydrogen barriers with stretched exponential fitting; output characteristics of TFTs with four cycles of hydrogen barrier; overlapped transfer curves of 10 self-aligned structured devices with four hydrogen barrier cycles; NBTS stability characteristics of self-aligned oxide TFT; and PBTS stability characteristics of the devices with two cycles of hydrogen barriers, which have similar initial V_{on} with the self-aligned structured device (PDF)

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Notes

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