

Engineering Negative Capacitance in $\text{Hf}_{0.5}\text{Zr}_{0.5}\text{O}_2$ for Low-Power and Reliable Charge Trap Flash Memory

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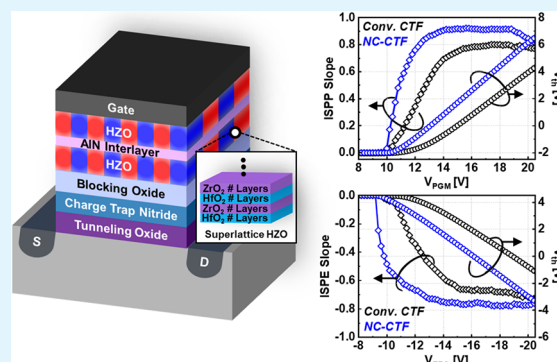
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Supporting Information

ABSTRACT: Charge trap flash (CTF) memory has emerged as a key solution for high-density nonvolatile memory. However, the high operating voltage of CTF memory leads to critical reliability issues, such as cell-to-cell interference and dielectric breakdown, limiting further pitch size scaling in 3D architectures. Here, we report a negative capacitance charge trap flash (NC-CTF) memory that exhibits remarkable operation efficiency by using the NC-induced capacitance boosting effect of $\text{Hf}_{0.5}\text{Zr}_{0.5}\text{O}_2$ (HZO) layer. To strengthen the NC effect and enable low-voltage program/erase (PGM/ERS) operations, we engineered the HZO layer by incorporating a dielectric interlayer (IL). The IL modulates the domain configuration within HZO, thereby enhancing the depolarization energy and stabilizing the NC state. Furthermore, adopting AlN as the IL material and employing a superlattice-based deposition process for HZO promoted the formation of oxygen vacancies and a spatial confinement effect, which collectively reduced the energy barrier for orthorhombic phase formation and enhanced ferroelectricity even at a halved thickness enabled by IL insertion. By embedding the engineered NC layer into the blocking oxide (BO), the NC-CTF achieves low voltage PGM/ERS operation while simultaneously addressing reliability concerns. These synergistic improvements pave the way for practical implementation of NC-CTF as a promising candidate for high-density, next-generation nonvolatile memory.

KEYWORDS: negative capacitance, HZO, superlattice, interlayer, charge trap flash, low power, reliability



1. INTRODUCTION

The continuous scaling of silicon-based CMOS technology has reached a plateau, with diminishing performance gains due to physical limitations such as short-channel effects, leakage currents, and thermal constraints.^{1,2} To transcend these challenges, the integration of novel device concepts is essential.^{3–5} Among various candidates, hafnia-based ferroelectrics have emerged as highly promising due to their outstanding CMOS compatibility and multifunctionality.^{6–8} Over the past decade, ferroelectrics have found broad applications in logic devices,^{9,10} nonvolatile memories (NVMs),^{11–15} power electronics,^{16–18} and computing-in-memory systems,^{19–22} positioning them as key enablers of next-generation electronics. Of the several emerging concepts linked to ferroelectrics, negative capacitance (NC), rooted in the distinct energy landscape of ferroelectrics, presents a particularly promising solution to address fundamental limitations in conventional electronic devices.^{23–26}

Although NC has been extensively investigated in phenomenological modeling,^{27,28} low-power transistor,^{9,29–31} and energy-related applications,¹⁷ its potential in nonvolatile memory remains largely underexplored. In this context, we integrated NC-induced capacitance boosting effect into the

blocking oxide (BO) of conventional CTFs to achieve performance improvements from a new perspective. NC-CTF inherits the operating mechanism of conventional CTF memory, where charge trapping and emission occur via the channel.^{32,33} The key distinction of NC-CTF lies in the dynamic modulation of the BO capacitance, wherein capacitance boosting occurs above a certain threshold voltage, thereby dramatically enhancing tunneling efficiency. Thus, the improvement of NC-CTF performance critically depends on the degree of NC-induced capacitance boosting and the operating voltage threshold at which it becomes effective, underscoring the importance of developing systematic engineering approaches to optimize these factors.

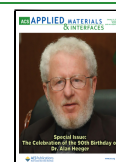
In this study, we present a combined experimental and modeling investigation to validate the enhancement of NC characteristics through modulation of the internal energy

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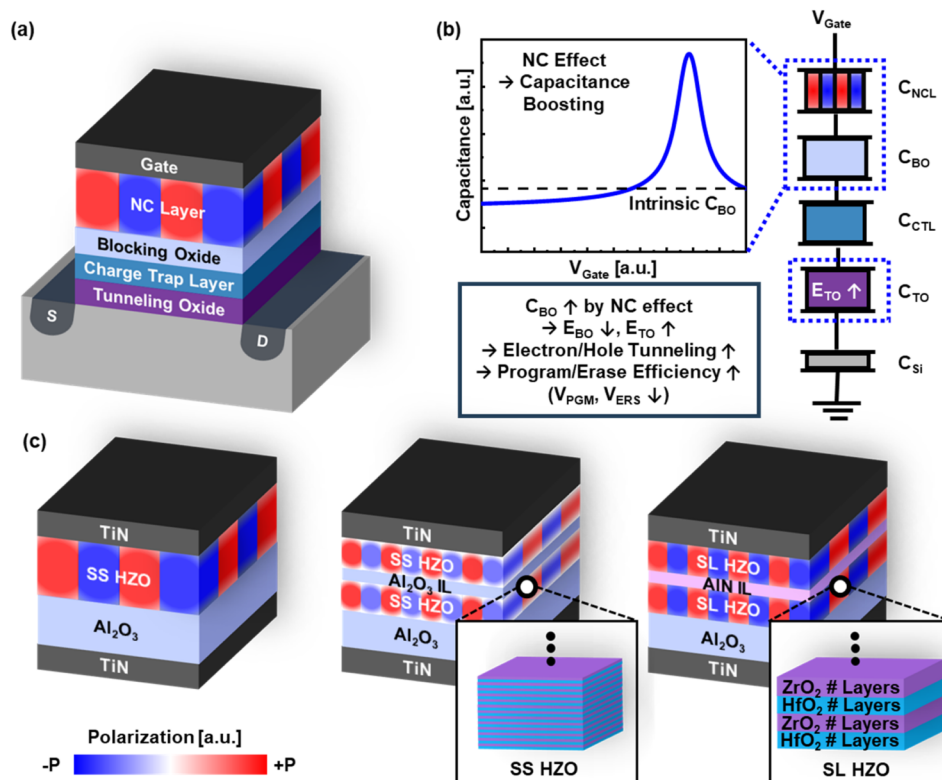


Figure 1. Overview of NC-CTF and strategies to enhance NC effect. (a) Schematic of NC-CTF memory. (b) Equivalent circuit of NC-CTF gate stack and concept of capacitance boosting by NC effect, which contribute to the high PGM/ERS efficiency. (c) Schematics of three different FE/DE bilayer configurations: SS HZO, SS HZO with an Al_2O_3 IL, and optimized SL HZO with an AlN IL.

landscape in HZO and to evaluate its impact on NC-CTF integration. We first analyze the interplay between depolarization energy and domain-wall energy in the multidomain configuration of the HZO layer, and employ 3D phase-field simulations to gain deeper insights into the underlying domain formation dynamics. Building on these insights, we design an HZO layer with an inserted AlN interlayer (IL-HZO), which not only enhances the depolarization energy but also mitigates the potential degradation of ferroelectric properties caused by IL insertion by optimizing the oxygen vacancy concentration within HZO. Furthermore, by adopting a $\text{HfO}_2/\text{ZrO}_2$ superlattice-based deposition strategy, we induce a confinement effect during the crystallization process, thereby stabilizing the orthorhombic phase even at reduced effective thicknesses and reinforcing the overall NC characteristics.

Leveraging these material-level improvements, we integrated the IL-HZO into the NC-CTF memory, which enabled substantial enhancement of PGM/ERS efficiency through the strengthened NC effect. This integration not only provided a wider memory window (MW) and reliable low-voltage operation, but also mitigated voltage-induced stress during repeated cycling. Consequently, the NC-CTF exhibited significantly improved endurance, retention, and stable PGM/ERS performance, establishing it as a promising candidate for next-generation nonvolatile memories.

2. RESULT AND DISCUSSION

2.1. Overview of NC-CTF

Figure 1(a) illustrates the structure of proposed negative capacitance charge trap flash (NC-CTF), where a negative capacitance layer (NCL) is integrated into a conventional CTF

memory gate stack consisting of a tunneling oxide (TO), charge trap layer (CTL), and BO. Figure 1(b) shows the corresponding equivalent circuit of the NC-CTF gate stack, highlighting the mechanism of reducing the operating voltage. The NC effect induces capacitance boosting of NCL/BO bilayer, which reduces the electric field across the BO while simultaneously increasing the electric field across the TO. This facilitates the active electron/hole tunneling at the TO and Si channel interface, leading to the improved PGM/ERS efficiency of the NC-CTF.

2.2. Strategies to Enhance NC Effect for NC-CTF

The NC effect arises from the depolarization field in the ferroelectric (FE) layer, and can be stabilized when the FE layer directly interfaces dielectric (DE) layer, owing to the unscreened polarization switching at the FE/DE interface and resulting energy modulation of the total system.^{27,34,35} In particular, the NC effect in multidomain ferroelectrics like HZO is governed by mechanisms distinct from those in single-domain systems, as internal domain interactions effectively suppress the depolarization field by alternating the direction of polarization switching.^{27,34,35} Accordingly, improving the NC effect in multidomain systems requires fundamentally different strategies from those employed in single-domain systems.

Enhancing the NC effect in multidomain HZO requires a clear understanding of its internal energy landscape. The equilibrium polarization state is dictated by the balancing between depolarization energy (f_{dep}) and domain wall energy (f_{dw}), whereby the system minimizes its total energy through their continuous adjustment. To amplify the NC effect, this interplay can be engineered such that f_{dep} increases more significantly under applied voltage. A key strategy for achieving

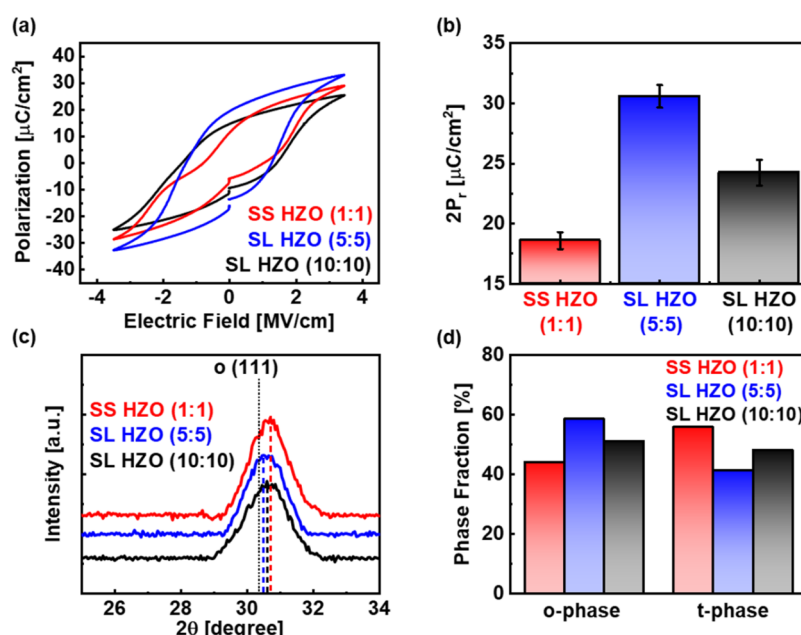


Figure 2. Comparative Analysis of Ferroelectric Properties in SS and SL HZO. (a) P–E hysteresis loops for 5 nm-thick HZO capacitors with different structures: SS HZO (1:1), SL HZO (5:5), and SL HZO (10:10). (b) Comparison of remanent polarization ($2P_r$) for the three HZO structures, highlighting the optimal value for the SL (5:5) configuration. (c) Grazing-incidence X-ray diffraction (GIXRD) spectra of the SS (1:1), SL (5:5) and SL (10:10) films. The dotted line marks the position of the ferroelectric orthorhombic (111) peak. (d) Quantitative phase fractions of the o- and t-phases derived from the deconvolution of GIXRD spectra.

this enhancement is to elevate the equilibrium f_{dw} , thereby providing a larger reservoir of energy that can be converted in to f_{dep} . Thickness scaling of HZO offers a practical route to this end. As the physical thickness of HZO decreases, the proximity of polarization charges intensifies the depolarization field, which destabilizes the system and drives the formation of denser domain configurations to restore energy balance.^{27,36,37} The resulting higher domain density increases the equilibrium f_{dw} , enabling its rapid conversion into f_{dep} under voltage application. Consequently, the accumulated f_{dw} is efficiently transformed into depolarization energy, yielding a stronger NC effect. The schematic of this energy conversion mechanism to enhance NC effect is depicted in Figure S1.

However, simple thickness scaling alone does not sufficiently consider the voltage distribution and effective charge boosting of FE/DE stack, which significantly influences the impact of NC effect. To simultaneously maintain the optimal HZO thickness regime (~ 10 nm)³⁶ for maximal charge-boosting efficiency and leverage the enhanced NC effect via internal energy modulation, we adopted a strategy of partitioning the physical HZO thickness by inserting an IL while preserving the total thickness. This enhancement of the NC effect through IL insertion is verified through both experimental measurements and 3D phase field simulations (Figure S2). However, as widely reported in previous studies,^{38,39} the reduction in HZO thickness and the integration of HZO with dielectric layers inevitably degrade its ferroelectric properties, posing a critical trade-off. This degradation was corroborated through the ferroelectric property analysis of the HZO separated by the IL (Figure S3).

Furthermore, we performed material optimization for both the HfZrO_2 (HZO) and the interfacial layer (IL) to mitigate the degradation of ferroelectricity that occurs upon IL insertion. Our analysis identified two primary challenges (Figure S4). First, to counteract the suppression of the critical orthorhombic (o-) phase in physically thin films, we replaced the conventional

solid-solution (SS) HZO with a superlattice (SL) HZO structure. The SL configuration stabilizes the o-phase through grain size engineering. Second, we addressed the further o-phase suppression induced by an Al_2O_3 IL—which reduces oxygen vacancies—by substituting it with an AlN IL. The AlN layer maintains a comparable dielectric constant with Al_2O_3 while improving the ferroelectricity of the HZO even with IL insertion.

These material engineering strategies are schematically illustrated in Figure 1(c), which compares three distinct FE/DE bilayer configurations: a baseline SS HZO, SS HZO with an Al_2O_3 IL, and our optimized SL HZO with an AlN IL. The diagrams, including zoomed-in insets showing the atomic layer deposition (ALD) process, depict how the resulting polarization strength (indicated by domain color brightness) varies with these material choices, culminating in an enhanced NC effect.

2.3. Determining the Optimal Cycle Ratio for Super-Lattice HZO

Stabilizing the ferroelectric o-phase in thin HZO is challenging due to nonuniform grain growth. SL HZO structures overcome this limitation, as their Zr-rich layers promote a more uniform grain size distribution that enhances o-phase formation.⁴⁰ However, a critical trade-off exists: excessively thick layers can inadvertently stabilize the nonferroelectric tetragonal (t-) phase of ZrO_2 and monoclinic (m-) phase of HfO_2 , degrading ferroelectric properties. Accordingly, we systematically optimized the SL cycle ratio to maximize the o-phase fraction.

To validate this optimization, we first investigated the polarization–electric field (P–E) characteristics of 5 nm-thick HZO capacitors with different cycle ratios (Figure 2(a)). The conventional SS HZO (1:1) reference sample showed low remanent polarization ($2P_r$) and a slanted hysteresis loop, indicative of significant nonferroelectric phase content. In contrast, the SL HZO structures exhibited substantially improved ferroelectricity. While both SL HZO (5:5) and

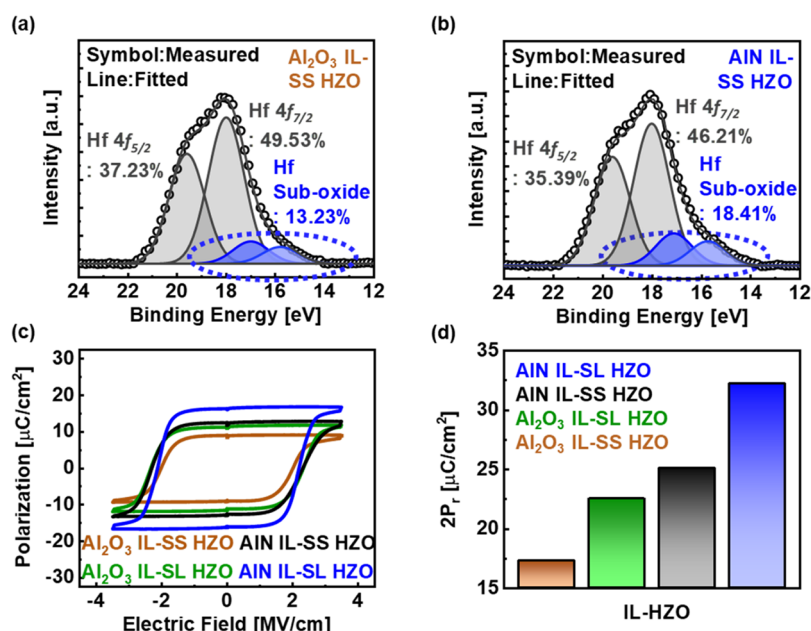


Figure 3. Electrical and material characterization of HZO with engineered ILs. (a), (b) X-ray photoelectron spectroscopy (XPS) analysis of the Hf 4f spectra for HZO films with Al₂O₃ and AlN ILs. Deconvolution of the spectra reveals a higher Hf suboxide fraction for the AlN IL, indicating an increased concentration of oxygen vacancies. (c) Positive-up-negative-down (PUND) measurements for four different device configurations, comparing SS and SL HZO with both Al₂O₃ and AlN ILs. (d) Summary of remanent polarization (2P_r) extracted from PUND data, demonstrating the optimal performance of the SL HZO and AlN IL combination.

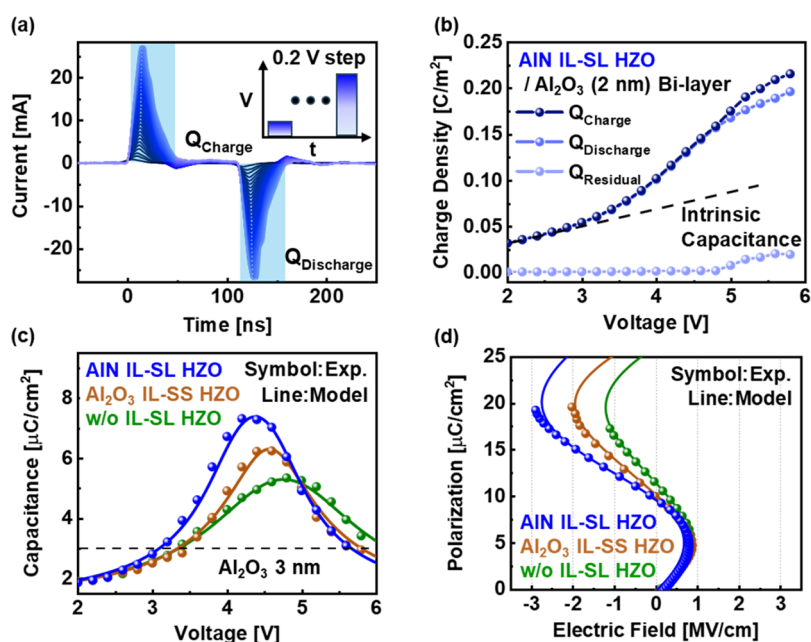


Figure 4. Enhancement of NC effect and capacitance boosting phenomenon in IL-HZO/Al₂O₃ bilayer. (a) Charging and discharging currents measured using a 100 ns incremental pulse technique, with the pulse scheme shown in the inset. (b) The resulting charge density–voltage (Q–V) curve for the optimized AlN IL-SL HZO bilayer. It shows a sharp, nonlinear increase in charge compared to the expected intrinsic capacitance (dashed line). (c) Capacitance–voltage (C–V) curves comparing the different bilayer structures. The experimental data (symbols) are fitted with the LGD model (solid lines). The fitting parameters used for the bilayer model are summarized in Table S1. The fully optimized AlN IL-SL HZO structure (blue) clearly shows the highest capacitance boosting. (d) P–E curves extracted for the single HZO layer within bilayer system. The region with a negative slope is direct evidence of NC, which explains the observed boosting.

(10:10) showed larger hysteresis loops, the (5:5) sample yielded a higher 2P_r, suggesting an optimal cycle ratio exists. The summary plot in Figure 2(b) confirms this trend, establishing the 5:5 cycle ratio as the most effective for enhancing ferroelectric properties.

To understand the physical origin of this electrical improvement, we performed grazing incidence X-ray diffraction (GIXRD) analysis. As shown in Figure 2(c), the SL HZO (5:5) sample exhibits the most pronounced o-phase-related peak near the o(111) position, whereas the SS HZO (1:1)

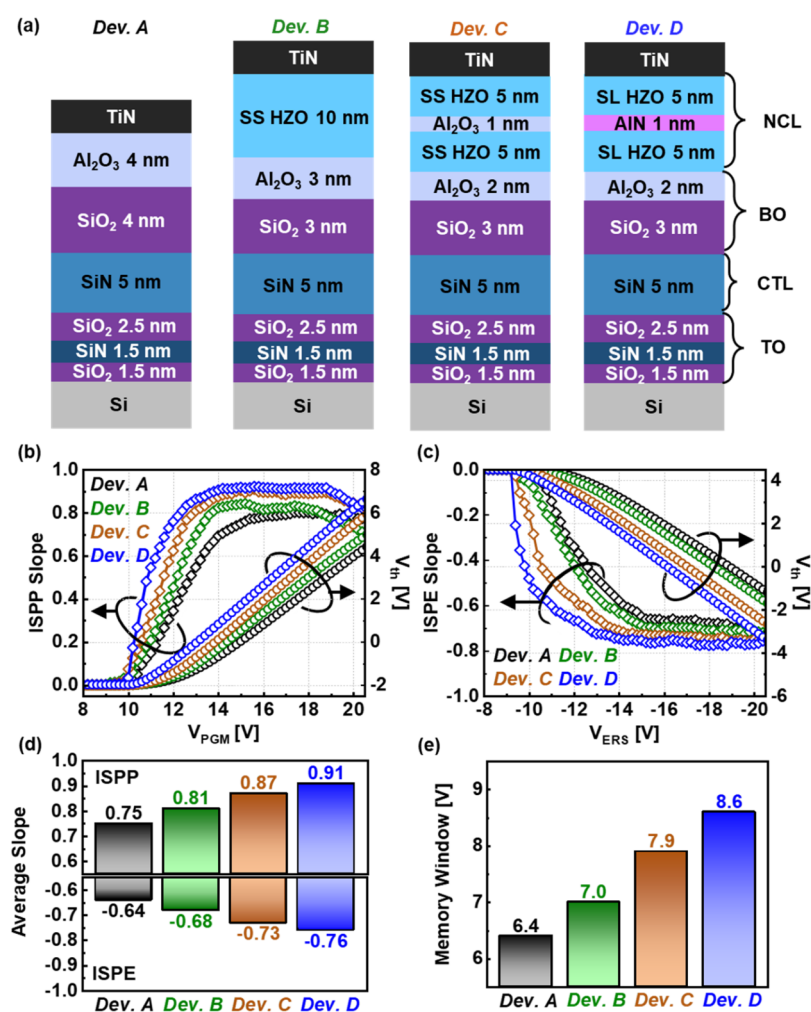


Figure 5. Program/erase performance and memory window (MW) of conventional CTF and NC-CTF. (a) Schematics of the four compared memory gate stacks: one conventional CTF (Dev. A) and three NC-CTF (Dev. B, C, D) devices featuring different Negative Capacitance Layers. (b) Incremental step pulse programming (ISPP) and (c) erasing (ISPE) characteristics, showing the V_{th} response to applied voltage pulses for each device. (d) Comparison of the average PGM/ERS slopes, which quantify efficiency. The NC-CTF devices are clearly more efficient than the Dev. A, with Dev. D exhibiting the steepest slopes. (e) The comparison of the MW for the conventional CTF and three NC-CTF memory devices within same PGM voltage region (8 ~ 20.5 V). The complete transfer I - V curves over the full voltage range are provided in the Figure S6.

sample shows the weakest o-phase signature. The SL HZO (10:10) sample shows an intermediate behavior between these two cases. Quantitative phase fraction analysis (Figure 2(d)) further reveals that the o-phase fraction follows the order SL HZO (5:5) > SL HZO (10:10) > SS HZO (1:1). Together, these consistent electrical and structural analyses demonstrate that the SL HZO (5:5) structure effectively enhances ferroelectricity, even at an aggressive thickness of 5 nm.

2.4. Influence of the IL on the Ferroelectric Properties of HZO

Next, we performed an analysis to assess the integrated ferroelectric properties upon inserting an IL into the HZO and to determine the influence of the IL material. The detailed evaluation methodology is described in Figure S4. Our analysis revealed that an Al₂O₃ IL degrades the ferroelectricity of HZO by suppressing the formation of oxygen vacancies at the HZO/Al₂O₃ interface, and an appropriate concentration of these vacancies is critical for stabilizing the ferroelectric o-phase.⁴¹

To overcome this degradation, we introduced an Aluminum Nitride (AlN) IL as a replacement. The AlN layer is advantageous for two reasons: (i) its aluminum component

can scavenge oxygen from HfO₂ due to a lower oxidation energy, creating the required vacancies; and (ii) its dielectric constant is similar to that of Al₂O₃, maintaining a comparable equivalent oxide thickness (EOT) and enabling a direct performance evaluation.

We correlated interfacial chemistry with electrical performance to understand the roles of the IL and HZO materials. X-ray photoelectron spectroscopy (XPS) analysis (Figure 3(a,b)) shows that the AlN IL promotes a higher concentration of oxygen vacancies at the interface compared to the Al₂O₃ IL, evidenced by a larger suboxide fraction in the Hf 4f spectra. PUND measurements (Figure 3(c,d)) confirm the functional impact of this change. While replacing either the Al₂O₃ IL with AlN or the SS HZO with SL HZO improved the remanent polarization ($2P_r$), the combination of SL HZO with an AlN IL demonstrated a synergistic effect, achieving the highest ferroelectric performance. This synergy arises because the AlN IL and SL HZO structure promote the ferroelectric o-phase through two distinct, complementary mechanisms.

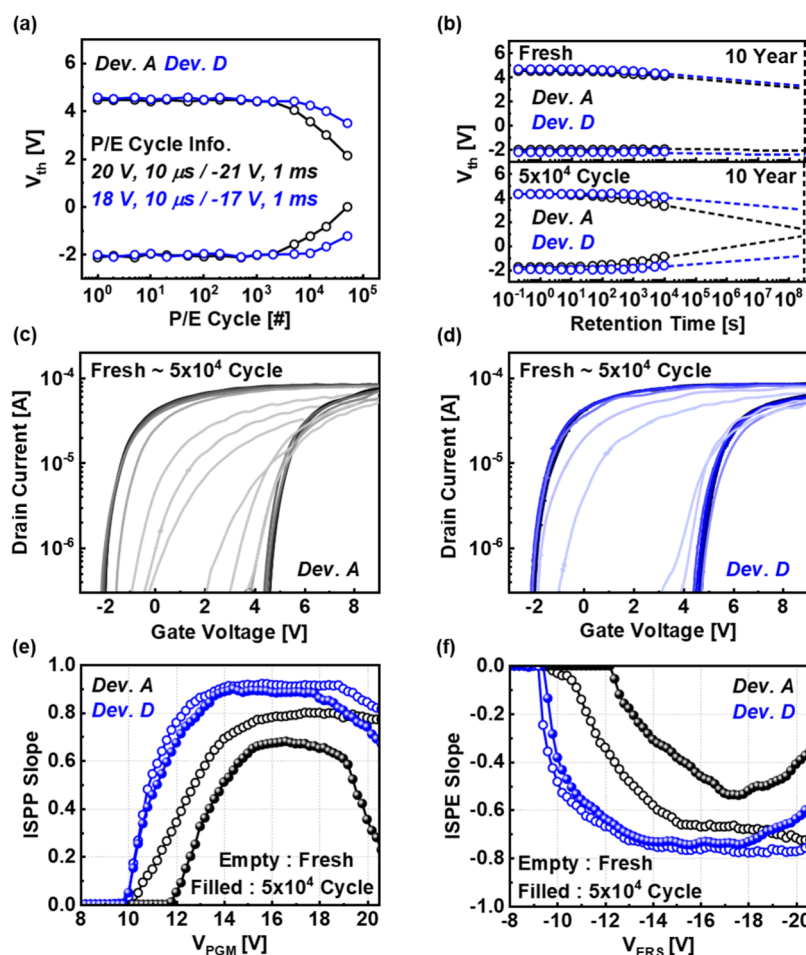


Figure 6. Reliability evaluation results of conventional CTF and AlN IL-SL HZO NC-CTF. (a) The enhanced endurance of Dev. D is attributed to its lower PGM/ERS voltages, which mitigate the electrical stress applied during repeated cycling, unlike the higher stress conditions for Dev. A. (b) The improved retention of Dev. D after PGM/ERS cycling is a direct consequence of the reduced electrical stress during repetitive operation, in contrast to the significant degradation observed in Dev. A. (c), (d) Comparison of pulsed I_{ds} – V_{gs} curves of Dev. A and Dev. D with from the fresh state to 5×10^4 PGM/ERS cycle. (e), (f) ISPP and ISPE characteristics of Dev. A and Dev. D before and after 5×10^4 P/E cycles. For a full view of the transfer I – V behavior under program and erase operation in both states, the complete I – V curves are provided in the Figure S9.

2.5. Capacitance Boosting Effect of the Engineered NC Layer

To investigate the capacitance boosting driven by the NC effect, we performed 100 ns short-pulse measurements on the engineered IL-HZO/ Al_2O_3 bilayer system. We first measured the charging and discharging currents under voltage pulses of increasing amplitude (Figure 4(a)) and integrated them to get the charge–voltage (Q – V) characteristics. Unlike a conventional dielectric's linear response, the optimized AlN IL-SL HZO bilayer shows a sharp, nonlinear increase in charge density around the applied voltage of 3 V (Figure 4(b)). This is the clear signature of capacitance boosting induced by the NC effect. By differentiating the Q – V curves, we obtained the capacitance–voltage (C – V) characteristics for each device configuration (Figure 4(c)). Using the Landau–Ginzburg–Devonshire (LGD) model to fit the data, we confirmed that all bilayers show capacitance enhancement over the capacitance of Al_2O_3 single layer. Notably, the fully optimized AlN IL-SL HZO structure exhibits the most significant boost, highlighting a powerful synergistic effect between our material and structural engineering strategies. As the definitive proof, we extracted the internal P–E behavior of HZO layer within bilayer system (Figure 4(d)).

The appearance of a negative electric field across the HZO layer provides direct physical evidence of the NC effect.

2.6. Integration of NC Layer in to a CTF Memory Stack

To validate the NC effect in a practical application, we integrated our engineered IL-HZO layers as NC layer (NCL) into CTF memory devices. As shown in Figure 5(a), we fabricated a conventional CTF device (Dev. A) as a control and three different NC-CTF devices (Dev. B to D) to compare their performance. A crucial aspect of our experimental design was to ensure a fair comparison; therefore, the BO thickness of each device was carefully adjusted to maintain an identical EOT. The detailed fabrication process is provided in Figure S5.

We evaluated the PGM performance using an incremental step pulse programming (ISPP) scheme, where PGM efficiency is quantified by the ISPP slope—the rate of V_{th} shift as the program voltage was ramped from 8 to 21 V. The ISPP characteristics in Figure 5(b) reveal a dramatic performance improvement for the NC-CTF devices. While the control device (Dev. A) required a high PGM voltage (over 20 V) to achieve a significant V_{th} shift, all the NC-CTF devices (Dev. B, C, and D) exhibited much steeper ISPP slopes, achieving large V_{th} shifts at substantially lower voltages. This significantly enhanced PGM

efficiency is a direct result of the capacitance boosting provided by the NCL.

This trend of improved efficiency continues in the ERS performance, where the NC-CTF devices again outperform the control (Figure 5(c)). A summary of the average PGM (ISPP) and ERS (ISPE) slopes (Figure 5(d)) provides a quantitative look at these gains. The NC-CTF devices consistently exhibit steeper slopes, which translates directly to the wider MWs observed in Figure 5(e). Notably, the fully optimized Dev. D (AlN IL-SL HZO) shows the highest PGM/ERS performance and the largest MW. This improved device performance strongly correlates with its superior capacitance boosting, which we demonstrated in the previous section. This correlation validates that our engineering strategies—using an optimized AlN IL and SL HZO—are highly effective for enhancing NC-CTF device performance.

2.7. Reliability of NC-CTF

A key advantage of NC-CTF devices is their potential for superior endurance, a critical reliability metric, due to enhanced PGM/ERS efficiency at lower operating voltages. This efficiency allows a target MW to be achieved with less electrical stress. To quantify this, we found that our optimized device (Dev. D) required significantly lower PGM/ERS voltages (PGM: 18 V, 10 μ s/ERS: -17 V 1 ms) to achieve a 6.5 V MW for triple-level cell (TLC) operation compared to the control device (Dev. A), which required (PGM: 20 V, 10 μ s/ERS: -21 V 1 ms) based on switching speed analysis of Figure S7. To validate the benefits of this reduced voltage, we conducted an endurance test as shown in Figure 6(a). It shows that Dev. D maintained a stable MW up to 1×10^4 cycles, whereas Dev. A's MW degraded noticeably beyond this point. Furthermore, after 5×10^4 PGM/ERS cycles, Dev. D preserved its data retention characteristics, while Dev. A suffered substantial retention loss (Figure 6(b)). This superior reliability is attributed to reduced physical degradation, as evidenced by the stable transfer curves of Dev. D after 5×10^4 cycles, in contrast to the significant degradation observed in Dev. A (Figure 6(c,d)). The robustness of Dev. D was further demonstrated by its stable PGM and ERS slopes, which remained consistent even after extensive cycling (Figure 6(e,f)). The detailed ISPP/ISPE behavior of the two devices under repeated PGM/ERS cycling is shown in Figure S8. This result affirms the strong correlation between the lower operating voltages enabled by the NC effect and the enhanced endurance of the device.

3. CONCLUSIONS

In summary, we have demonstrated a novel and synergistic strategy to engineer the NC effect for high-performance memory applications. By physically partitioning a HZO layer with an engineered IL, we created a new pathway to amplify the depolarization energy, thereby maximizing the NC effect. This was further enhanced by optimizing the material properties, where a combination of a SL HZO structure and an AlN IL synergistically stabilized the ferroelectric phase. When integrated into a CTF memory device, this optimized structure led to substantial performance gains. We achieved a significant reduction in PGM/ERS voltages and a corresponding expansion of the MW. Crucially, the lower operating voltage directly translated to enhanced device reliability, as evidenced by superior endurance and retention characteristics. These findings establish a powerful codesign methodology involving depolarization energy engineering and ferroelectric property tuning.

This work not only provides a solution for overcoming the scaling challenges of conventional NAND flash but also opens new avenues for designing advanced ferroelectric devices. Future efforts will build upon this foundation to further push the limits of scalability and energy efficiency in next-generation memory technologies.

4. EXPERIMENTAL SECTION

4.1. Device Fabrication

The IL-HZO/Al₂O₃ bilayer was fabricated on a Si/SiO₂ substrate. A 100 nm TiN bottom electrode was deposited via DC sputtering. The HZO, Al₂O₃, and AlN layers were subsequently deposited using plasma-enhanced atomic layer deposition (PEALD) at 320 °C. TEMA₂Hf, TEMA₂Zr, and TMA were used as the Hf, Zr, and Al precursors, respectively. The HZO and Al₂O₃ layers were deposited using O₂ plasma, while AlN was formed using NH₃ plasma. A 50 nm TiN top electrode was then deposited using the same sputtering process. Following top electrode patterning, the devices underwent rapid thermal annealing (RTA) at 600 °C for 10 s in an N₂ atmosphere to enhance crystallization.

For CTF fabrication, a 550 nm field oxide layer was thermally grown on APM-cleaned Si and active area was patterned. The replacement gate was then formed, and the source/drain regions were defined through ion implantation, followed by activation at 1000 °C for 30 s in an N₂ ambient. After activation, the gate stack process was conducted, as detailed in Figure S5.

4.2. Device Characterization

The electrical characteristics of the HZO capacitor, IL-HZO bilayer, and CTF memory devices were measured using a Keithley 4200A-SCS and a device current waveform analyzer (CX3324A, Keysight). For short-pulse measurements, a pulse generator (81104A, Keysight) was used to apply the required voltage pulses.

For phase analysis of SS and SL HZO, GIXRD analyzer (Rigaku, SmartLab) was employed. To investigate the composition of HZO in the IL-HZO bilayer XPS (Thermo Fisher Scientific, K- α) analyze was conducted.

■ ASSOCIATED CONTENT

SI Supporting Information

The Supporting Information is available free of charge at <https://pubs.acs.org/doi/10.1021/acsami.5c18930>.

Details of three-dimensional phase-field simulations for HZO, PUND measurement procedures for evaluating IL-inserted HZO, process flow of device fabrication, additional data on switching speed comparison among devices, complete transfer *I*–*V* characteristics for all devices, average ISPP/ISPE slopes under repeated P/E cycling, fitting parameters for the negative capacitance analysis (PDF)

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Notes

The authors declare no competing financial interest.

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