Trench-Structured High-Current-Driving Aluminum-Doped Indium–Tin–Zinc Oxide Semiconductor Thin-Film Transistor

Do Hyung Kim, Kwang-Heum Lee, Seung Hee Lee, Junsung Kim, Junghoon Yang, Jingyu Kim, Seong-In Cho, Kwang Hwan Ji, Chi-Sun Hwang, and Sang-Hee Ko Park

***Abstract*— This letter presents a thin-film transistor architecture, in which a "trench" is introduced between the source and drain electrode to enhance current flow. The top-gate top-contact oxide Trench thin-film transistor has a superior on-current per width of 27.7 μA/μm at a drain voltage of 4.1 V. It also has a good subthreshold swing of 0.122 V/dec and turn-on voltage of −0.4 V. This study explores the operating mechanism of the high-current-driving Trench oxide thin-film transistor.**

***Index Terms*— Aluminum-doped indium–tin–zinc oxide, on-current boosting effect, oxide semiconductor, thin-film transistor, trench structure.**

I. Introduction

OXIDE semiconductor thin-film transistors (TFTs) are considered to be promising candidates for next-generation displays because of their high mobility [1], [2], low leakage current, and improved uniformity and stability [2], [3]. Despite these advantages, certain problems, such as reduced pixel charging time and limited space per pixel, must be addressed for their application in ultrahigh-resolution displays. To this end, small-sized oxide TFTs should have high current driving ability. Oxide TFTs with high mobility and high driving current have been widely investigated [4], [5]; however, the deterioration of electrical characteristics arising with downscaling of the device size was not considered in these studies [6], [7], [8], [9]. Oxide vertical TFTs have also been researched for achieving high on-current in a small size [10], [11], [12]. These devices, however, require complex fabrication processes resulting in problems like voids and shadowing, in addition to the degradation of the subthreshold swing (SS).

Herein, we propose a high-performance oxide TFT with a simple device architecture, i.e. a trench structure. The "Trench TFT" fabricated with a top-gate top-contact (TGTC) structure with 5.46 μm short channel has an ultrahigh on-current per unit width that reaches ~27.7 μA/μm at a drain voltage (V_{DS}) of 4.1 V. Moreover, the Trench TFT shows a good SS of 0.122 V/dec, which is low enough to be comparable to that of a conventional planar TFT, and V_{on} value close to zero (−0.4V). We also scrutinize the unique operation mechanism of the Trench oxide TFT and its excellent electrical properties.

II. Experimental

Fig. 1(a) shows the schematics of TGTC planar and Trench TFTs, and Fig. 1(b) shows the fabrication workflow of the Trench TFT. In the Trench TFT fabrication, a 214-nm-deep trench was formed by photolithography and reactive ion etching (RIE) on a silicon wafer with a 500-nm-thick thermally grown SiO_2 buffer layer. Subsequently, an aluminum-doped indium–tin–zinc oxide (Al-ITZO) active layer was deposited to a thickness of 17.5 nm by radio frequency (RF) sputtering. Next, a 150-nm-thick molybdenum layer was deposited by direct current (DC) sputtering as the source and drain electrodes. After that, a 35-nm-thick Al_2O_3 layer of gate insulator (GI) was deposited by plasma-enhanced atomic layer deposition (PEALD) at 200 °C using a trimethylaluminum source. Finally, a 150-nm-thick molybdenum layer was deposited by DC sputtering as the gate. All the deposited thin-film layers were patterned via photolithography and wet etching. For direct comparison with the Trench TFT, a conventional planar TFT without the trench was fabricated simultaneously on the same substrate. Post-annealing was performed first at 200 °C, then at 230 °C, and finally at 250 °C, cumulatively for 2 h each, in a vacuum.

For the active thickness splitting, planar and Trench TFTs with an Al-ITZO active layer of 4.4 nm/8.7 nm/26.1 nm/35.2 nm/52.5 nm were additionally fabricated. Among these, the planar TFT with an active thickness of 4.4 nm showing switching property was chosen as the counterpart of the Trench TFT with a 17.5 nm active layer to compare the electrical properties. Their fabrication conditions were the same as those described above, except the active layer thickness. The devices with 4.4 nm active thicknesses were post-annealed at 200 °C

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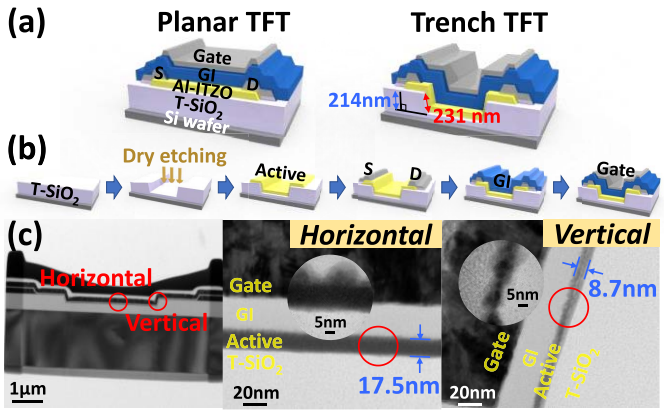

Fig. 1. (a) Schematics of TGTC TFTs showing the planar and Trench structures. (b) Fabrication workflow of the Trench TGTC TFT. (c) TEM images of the Trench TFT.

and then 280 °C, cumulatively for 2 h each, in a vacuum, whereas those with thicknesses of 8.7 nm, 26.1 nm, 35.2 nm, and 52.5 nm were post-annealed at 200 °C and then 230 °C.

The electrical properties of the devices were investigated using an HP-4156A semiconductor parameter analyzer under ambient conditions.

III. Results and Discussion

Fig. 2(a) shows the I–V characteristics of the planar and Trench TFTs (17.5-nm-thick active layers). Whereas the planar TFT showed conductive properties during the gate voltage (V_G) sweep, the Trench TFT showed switching properties. The transmission electron microscopy (TEM) images of Trench TFT (Fig. 1(c)) show that the active layer thickness on the trench sidewall was 50% lower than that on the horizontal region. This originated from the anisotropic characteristic of the sputter equipment used to deposit the active layer. The electrical properties of an oxide semiconductor TFT depend significantly on the total number of carriers in the semiconductor. With decreasing thickness of the active layer, the turn-on voltage (V_{On}) shifts positively and the channel resistance increases, owing to the decrease in the total number of carriers [13], [14], [15], [16]. Thus, while a TFT with a thick active layer becomes conductive, a TFT with a thinner active layer results in a well-operating TFT.

The thin-film stacking sequence and fabrication conditions for the horizontal part of the Trench TFT were similar to those of planar TFTs. Accordingly, the horizontal part exhibited conductive properties as seen in the planar TFT (Fig. 2(a) and Fig. 2(b)). The carrier concentration of the Al-ITZO channel was 3.090E+21 cm^{-3} in the planar TFT, and 1.658E+21 cm^{-3} in the horizontal part of the Trench TFT, showing that both had highly conductive properties. Thus, it can be inferred that only the short vertical parts of the active layer act as the effective channels that show the switching property. Meanwhile, the conductive horizontal part of the thicker section acts as a fast-current path boosting the on-current. This finding could be verified by the output characteristics which exhibited similar current levels despite the channel length variation (Fig. 2(c)), since the effective channel length (462 nm) of the two vertical channels remained constant. Meanwhile, the variation of the on-current with the channel width of the Trench TFTs followed the typical trend of the I–V characteristics.

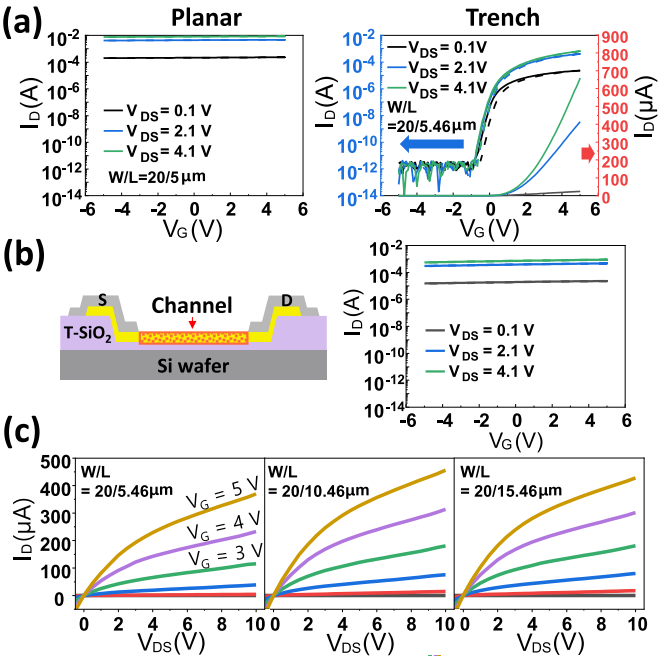

Fig. 2. (a) Transfer characteristics of the TGTC planar and Trench TFTs with an Al-ITZO active layer of thickness 17.5 nm. The solid line represents forward sweeping, and the dotted line represents reverse sweeping. (b) Cross-sectional schematic of the TGTC Trench TFT for measuring the electrical properties of only the horizontal active part, and the corresponding transfer curve. $W/L = 160\ \mu m/160\ \mu m$. (GI and gate are omitted) (c) Output curves of the Trench TFTs with channel lengths of 5.46, 10.46, and 15.46 μm.

For further research, active thickness splitting was performed. Fig. 3(a) presents the transfer curves of the planar and Trench TFTs with various horizontal region active thicknesses, and Fig. 3(b) depicts their on/off characteristics. The active thickness of the Trench TFT in Fig. 3(b) corresponds to that of the vertical part, which determines the on/off characteristic of the TFT. The Trench TFT had a serial connection of planar and vertical TFTs (Fig. 3(c)). Therefore, the on/off characteristics were expected to be similar between planar and Trench TFTs with the same determining active thickness. However, this was not to case (Fig. 3(b)). Consequently, this infers that some factors other than the active thickness influence the on/off characteristics of Trench TFTs.

Roughness of the vertical part also contributed to the large difference between the vertical and the horizontal parts. Fig. 4 shows a scanning electron microscopy (SEM) image of a trench with a photo resist and its schematic. During the RIE process, the collision of F^- plasma ions produced many dangling bonds, which acted as trap sites on the surface of the thermal SiO_2 buffer layer [17], [18]. Moreover, the ions bombarded the buffer layer owing to Coulombic force, resulting in directionality. Therefore, the topology of the sidewall was formed with the same shape as the photoresist edge [19]. Technical limitations of the photolithography equipment and the photo resist prevented formation of a smooth resist edge (rough edge in Fig. 4), resulting in roughness on the sidewall. This can also be seen in Fig. 1(c), vertical, in a blurred superimposed form.

The rough back surface obstructed the carrier path in the vertical channel, increasing the probability of carrier trapping [20], [21]. Additionally, since the active layer was sufficiently thin, a rough interface was also formed between the active

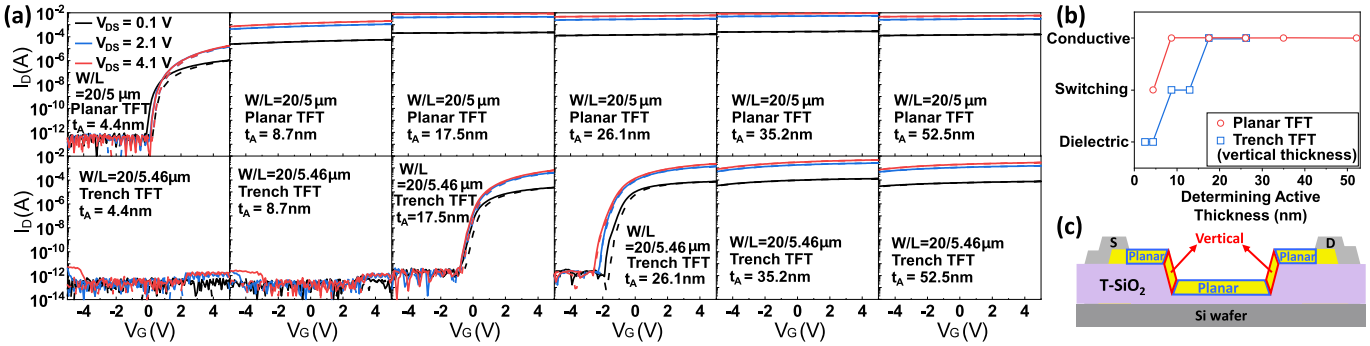

Fig. 3. (a) Transfer curves of the TGTC planar and Trench TFTs with active thicknesses (t_A) of 4.4, 8.7, 17.5, 26.1, 35.2, and 52.5 nm. (b) The on/off characteristics of the curves in (a) are summarized. (c) The Trench TFT consists of a serial connection of planar/vertical/planar/vertical/planar TFTs. GI and gate layers have been omitted.

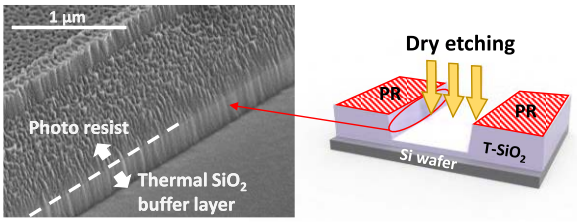

Fig. 4. SEM image of the trench hole with photo resist.

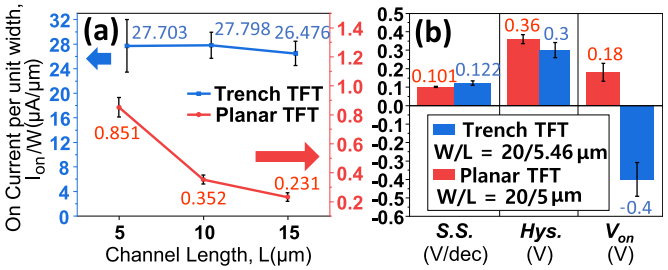

Fig. 5. (a–b) Electrical properties of the planar TFTs with 4.4 nm-thick Al-ITZO active layers and the Trench TFTs with 17.5 nm-thick ones. V_{DS} = 4.1 V. (a) The normalized on-current. (b) Comparison of SS, hysteresis, and V_{On} between the planar and Trench TFTs.

layer and the GI. This topology reduced the mean-free-time of free electrons by interfering with their movement. Therefore, the carrier mobility would be lowered according to the following equation [22]:

$$\mu = \frac{e\tau_c}{m^*}, \tag{1}$$

where e is the electron charge, τ_c is the mean-free-time of the electron, and m^* is the effective mass. Since the channel resistance (R_{Ch}) is inversely proportional to the mobility [22], the decrease in mobility increased the channel resistance. The channel resistance of the vertical channel could be calculated as [23]:

$$\begin{aligned} R_{Tot,Trench} &= \frac{V_{DS}}{I_D} = R_{Ch} + R_C \\ &= (R_{Ch,horizontal} + 2R_{Ch,vertical}) + R_C, \end{aligned} \tag{2}$$

$$R_{Tot,planar} = \frac{V_{DS}}{I_D} = R_{Ch} + R_C = R_{Ch,horizontal} + R_C, \tag{3}$$

where R_{Tot}, I_D, R_{Ch}, and R_C represent the total resistance, drain current, channel resistance, and contact resistance respectively. The channel resistance of the 8.7-nm-thick vertical channel in the Trench TFT was 2868 Ω at V_{DS} of 4.1 V and V_G of 5 V. This value is 2.20 times higher than that of the planar TFT (1306 Ω) with the same active thickness of 8.7 nm. Consequently, the roughness contributed to the difference between the vertical part and the horizontal part by increasing channel resistance on the vertical part.

Fig. 5(a) shows normalized on-currents of the planar TFT with a 4.4-nm-thick active layer and the Trench TFT with a 17.5-nm-thick active layer. Due to the extremely short effective channel (462nm), the normalized on-current of the Trench TFT with a channel length of 15.46 μm reaches 26.5 μA/μm at V_{DS} of 4.1 V. Notably, it remains without degradation even with a short channel length. The normalized on-current of the Trench TFT with a channel length of 5.46 μm was 27.7 μA/μm at V_{DS} of 4.1 V. Fig. 5(b) shows the typical electrical properties of the planar and Trench TFTs. The Trench TFT also had a good SS of 0.122 V/dec. This value is sufficiently low and comparable to that of the planar TFT (0.101 V/dec) and is the lowest among oxide TFTs with vertical channels [10], [11], [12], [24], [25]. Moreover, it had acceptable V_{On} close to zero (−0.4 V). Additionally, it had better positive-bias temperature stress (PBTS) stability (threshold voltage shift (ΔV_{Th}) of 1.33 V for 10000 s) than the planar TFT (ΔV_{Th} of 1.66 V) when the channel footprint was W/L = 40 μm/20 μm (data not shown).

IV. Conclusion

TFTs with a "Trench structure" were proposed to meet the requirements for ultra-high resolution. The normalized on-current of the Trench TFT, even with short channel footprint, reached as high as 27.7 μA/μm. Additionally, it exhibited good SS and V_{On} values. The vertical active layers acted as the effective channels owing to the higher channel resistance, while the conductive horizontal part acted as the current path leading to a high on-current. Trench TFTs are advantageous in terms of process efficiency due to fabrication compatibility with existing planar TFTs. However, further process improvement is needed to increase uniformity on large areas. The obtained advanced electrical properties indicate that the oxide Trench TFTs can replace low-temperature polycrystalline silicon (LTPS) TFTs in mobile display backplanes and play a critical role in next-generation extended-reality displays.

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